XEROX

PALO ALTO RESEARCH CENTER

3333 Coyote Hill Road
Palo Alto, California 94304
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To: MPC79.distribution

From: The MPC79 Organizers

Subject: **Message #1: Information and Schedules for MPC79**

Filed on: [MAXC] < Conway > MPC79.memo1

GREETINGS!

This is message #1 of a series of messages about the fall 1979 multi-university multiproject chip set (MPC79). A large number of LSI design projects from several universities will be simultaneously implemented in this chip-set. As of now the participating universities are: MIT, Caltech, Stanford, Univ. of Rochester, CMU, and U.C.Berkeley. We may possibly include projects from a few other universities.

This effort has two main purposes: First, it will enable a lot of students and university researchers to have their projects implemented very quickly (we estimate the total turnaround time from design cutoff to packaged chips will be ~4 weeks). Second, it will provide a test of the prototype software and operational procedures we are using to provide this remote-entry, fast-turnaround implementation service.

There are no charges for participation: information management is being provided and maskmaking is being funded by Xerox Corporation; message and design file communication services are being supported by use of the ARPANET; wafer fabrication is being provided by Hewlett-Packard; packaging services will be provided by the universities.

This message provides information about the participating universities and the organizations supplying the implementation service, identifies the design file format, the process, the design rules, and the value of lambda, gives a tentative estimate of the available average space per project, sets certain key dates in the chip-set schedule, lists some tasks to be done by the project lab coordinators, and lists some things to watch for in future messages.

These informational messages are being sent to instructors and project lab coordinators in the universities, and also to those in the ARPA VLSI community who might be interested in following the progress of MPC79. Requests for additions or deletions to the message distribution list, requests for information about MPC79, and all requests for service or status by participants should be communicated by electronic messages via the ARPANET to MPC79@PARC-MAXC.

1. THE PARTICIPATING UNIVERSITIES:

MIT: Course 6.371; Jonathan Allen, instructor; Randy Bryant, TA; 30 students; we estimate that this course will produce 20 projects. We may also include several research prototype designs by MIT faculty members and research staff members.

Caltech: CS/EE181a; Douglas Fairbairn, instructor; Greg Eflan, Dick Lang, TA's; 43 students; estimate 30 projects.

Stanford University: EE292V; Rob Mathews and John Newkirk, instructors; 71 students + 40 auditors; 1st quarter of 2-qtr sequence; most students will complete projects in 2nd qtr; however, we plan to include in MPC79 those students projects completed by the MPC79 cutoff date; we also plan to include some research-prototype designs by Stanford faculty/research staff members; estimate 15 projects.

University of Rochester: EE492/CS492; being taught by a group of EE and CS faculty; Mark Kahrs, TA; 14 students; estimate 10 projects.

Carnegie-Mellon University: Bob Sproull's course is offered in the spring. However, 6 to 8 research prototype designs by CMU faculty members and grad students will be included in MPC79.

U.C.Berkeley: Carlo Sequin's course, CS248, is offered in the winter quarter. However, we plan to include several research-prototype designs by Berkeley faculty members and grad students.

2. ORGANIZATIONS INVOLVED IN IMPLEMENTING MPC79:

Information management for the chip-set will be provided by members of the LSI Systems Area of the Xerox Palo Alto Research Center (PARC), Palo Alto, California. Xerox PARC staff members will (i) support the message and design-file transfer interactions with the university project labs, (ii) provide the technical information necessary for participation, (iii) define the "rules of the game" for space allocation and scheduling, (iv) interact with the various project labs to debug the procedures for interaction well in advance of the final design cutoff date, (v) accept the data files for completed designs, and then (vi) on the cutoff date convert and merge all the designs into mask specifications, and then coordinate maskmaking, wafer fabrication, dicing, and the shipment of wafers/chips back to the universities.

Electronic message service and LSI design file transmissions will be supported by use of the ARPANET. The ARPANET is being used by Xerox PARC and the major universities, all of which are ARPA contractors, to further test the use of such networks for organizing and operating remote-entry, fast-turnaround implemention of large numbers of integrated system designs (an initial feasibility test was made last year in support of the fall '78 MIT course).

Maskmaking for MPC79 will be done by Micro Mask, Inc., Sunnyvale, CA, using an ETEC electron-beam maskmaking system.

Wafer fabrication for MPC79 will be done by Hewlett-Packard at the HP Deer Creek Research Laboratory, Palo Alto, CA, using an nMOS, depletion-load, silicon-gate process.

Packaging: Wafers will be diced at PARC. The chips will be returned to the universities for mounting and custom wire-bonding (we'll send more info about packaging in later messages). Some schools have inadequate wire-bonding facilities, and a limited amount of wire-bonding may possibly be provided by PARC for those schools; we'd like to hear from other schools or firms that could help provide this wire-bonding support.

3. DESIGN FILE FORMAT; PROCESS; DESIGN RULES;
   VALUE OF LAMBDA:

DESIGN FILE FORMAT: CIF2.0, as documented in "Introduction to VLSI Systems", by Mead & Conway, Chapter 4; PROCESS: nMOS, depletion-load, silicon-gate process; DESIGN RULES: Mead & Conway (see Ch. 2 and Color Plates 3 and 4 in "Introduction to VLSI Systems"); LAMBDA = 2.5 microns.

4. AVERAGE SPACE PER PROJECT:

Here are some very preliminary estimates: The total number of projects will be ~ 60 to 100. We are planning to produce two E-beam mask sets, with each mask set containing five to seven different multiproject chip types, with each chip being ~ 6mm by 6mm. Thus, the average student project should be ~ 2mm by 2mm. If a university class wants to send some very big projects, they should plan to compensate by sending some small ones to keep the average size down. [We will soon provide a library of cells, including input and output pads that have a pitch of ~106 lambda. Thus at lambda = 2.5 microns, even a 2mm by 2mm project can have ~7 pads on a side, and can contain quite a lot of stuff.]

We are very interested in supporting serious university research projects with these MPC efforts (such as the recent LISP machine chip designed by Sussman, Holloway, Bell, and Steele). Separate consideration for space allocation will be given for such projects.

5. SOME KEY DATES (these are firm deadlines):

(i) Each school should confirm, by no later than 13 November, that the actual software and hardware to be used for final design file transmission to MAXC is operating correctly. This should be done by placing the CIF design file of a typical moderate-sized design on MAXC (the design doesn't need to be in finished form, and doesn't need to be one intended for MPC79, but it should contain a representative collection of CIF primitives and symbols for the purpose of testing the overall system), and then mailing a checkplot of the same file to Lynn Conway, Xerox PARC, 3333 Coyote Hill Road, Palo Alto, CA 94304. We will plot the file here and compare plots to see if the transmission was successful, the CIF code was valid, etc.

(ii) Preliminary "final" versions of all projects must be submitted no later than 27 November. The final space allocation will be made at this time, with those designs earliest to reach the appearance of final form receiving the highest priority. There will be one week remaining to check for errors and resubmit corrected versions before the design cutoff date. However, dimensions of projects may not increase after this time without risk of losing their space allocation.

(iii) The design cutoff date/time will be 4 December at 5:00pm PST. All accepted projects will be gathered at that time and merged into the mask specifications.

6. SOME THINGS TO DO:

(i) Each school should designate some person(s) to be the project coordinator(s). The coordinator

will relay the MPC79 message information, "rules of the game", etc. to those doing design projects at their school, will interact with MPC79 to set-up and test the file-transmissions procedure from their school, and later-on will interact with MPC79 via messages and file transfers to submit design files for inclusion in the chip-set.

(ii) A MAXC account < universityname-VLSI > has been established at PARC for each of the major participating universities to use for MPC79 design file transfers. The project lab coordinator(s) at each university should select a new password for their university's MAXC account, and notify us of that password (we will put it into effect immediately upon receipt). Also, please message the names of the coordinators, and the names of those who will know the MAXC password.

(iii) We will soon begin to make a gross allocation of space between the various schools, so as to provide you all with better estimates of available space. Later-on we'll make firm space allocations to individual projects, with preference given to those projects that are earliest to reach a near-finished form. Coordinators should keep MPC79 updated on the number of projects likely to be submitted by their university. If a school plans to submit several very large designs, let us know as soon as possible, with estimates of the project sizes. If a school expects to submit fewer designs than the estimates listed in item 1 above, please let us know (we can then make the space available to additional participants).

7. THINGS TO WATCH FOR IN COMING MESSAGES:

Message#2 (~ OCT 17): A small library of useful cells and the procedures for obtaining the library design files will be described.

Message#3 (~ OCT 22): The Request-Acknowledge form of interactions will be described for placing design files for checking and for submitting/resubmitting design files for merging into MPC79.

We welcome the students in the courses to the new and rapidly growing community of integrated system designers and researchers. There's a lot virgin territory for you to explore where few have worked before - it's very likely that some of you will discover important new architectural techniques or gain insight into important new research problems while working on your first design projects. We look forward to the excitement of the final month of project activity later this fall. If you have any questions, send us a message.

The MPC79 Organizers,

Lynn Conway, Alan Bell, Martin Newell, Dick Lyon
LSI Systems Area, Xerox PARC
12 October 1979