MPC79 Informational Messages:

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
October 12, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **Message #1: Information and Schedules for MPC79**

Filed on: [MAXC] < Conway > MPC79.memo1

GREETINGS!

This is message #1 of a series of messages about the fall 1979 multi-university multiproject chip set (MPC79). A large number of LSI design projects from several universities will be simultaneously implemented in this chip-set. As of now the participating universities are: MIT, Caltech, Stanford, Univ. of Rochester, CMU, and U.C.Berkeley. We may possibly include projects from a few other universities.

This effort has two main purposes: First, it will enable a lot of students and university researchers to have their projects implemented very quickly (we estimate the total turnaround time from design cutoff to packaged chips will be ~4 weeks). Second, it will provide a test of the prototype software and operational procedures we are using to provide this remote-entry, fast-turnaround implementation service.

There are no charges for participation: information management is being provided and maskmaking is being funded by Xerox Corporation; message and design file communication services are being supported by use of the ARPANET; wafer fabrication is being provided by Hewlett-Packard; packaging services will be provided by the universities.

This message provides information about the participating universities and the organizations supplying the implementation service, identifies the design file format, the process, the design rules, and the value of lambda, gives a tentative estimate of the available average space per project, sets certain key dates in the chip-set schedule, lists some tasks to be done by the project lab coordinators, and lists some things to watch for in future messages.

These informational messages are being sent to instructors and project lab coordinators in the universities, and also to those in the ARPA VLSI community who might be interested in following the progress of MPC79. Requests for additions or deletions to the message distribution list, requests for information about MPC79, and all requests for service or status by participants should be communicated by electronic messages via the ARPANET to MPC79@PARC-MAXC.

1. THE PARTICIPATING UNIVERSITIES:

MIT: Course 6.371; Jonathan Allen, instructor; Randy Bryant, TA; 30 students; we estimate that this course will produce 20 projects. We may also include several research prototype designs by MIT faculty members and research staff members.

Caltech: CS/EE181a; Douglas Fairbairn, instructor; Greg Eflan, Dick Lang, TA's; 43 students; estimate 30 projects.

Stanford University: EE292V; Rob Mathews and John Newkirk, instructors; 71 students + 40 auditors; 1st quarter of 2-qtr sequence; most students will complete projects in 2nd qtr; however, we plan to include in MPC79 those students projects completed by the MPC79 cutoff date; we also plan to include some research-prototype designs by Stanford faculty/research staff members; estimate 15 projects.

University of Rochester: EE492/CS492; being taught by a group of EE and CS faculty; Mark Kahrs, TA; 14 students; estimate 10 projects.

Carnegie-Mellon University: Bob Sproull's course is offered in the spring. However, 6 to 8 research prototype designs by CMU faculty members and grad students will be included in MPC79.

U.C.Berkeley: Carlo Sequin's course, CS248, is offered in the winter quarter. However, we plan to include several research-prototype designs by Berkeley faculty members and grad students.

2. ORGANIZATIONS INVOLVED IN IMPLEMENTING MPC79:

Information management for the chip-set will be provided by members of the LSI Systems Area of the Xerox Palo Alto Research Center (PARC), Palo Alto, California. Xerox PARC staff members will (i) support the message and design-file transfer interactions with the university project labs, (ii) provide the technical information necessary for participation, (iii) define the "rules of the game" for space allocation and scheduling, (iv) interact with the various project labs to debug the procedures for interaction well in advance of the final design cutoff date, (v) accept the data files for completed designs, and then (vi) on the cutoff date convert and merge all the designs into mask specifications, and then coordinate maskmaking, wafer fabrication, dicing, and the shipment of wafers/chips back to the universities.

Electronic message service and LSI design file transmissions will be supported by use of the ARPANET. The ARPANET is being used by Xerox PARC and the major universities, all of which are ARPA contractors, to further test the use of such networks for organizing and operating remote-entry, fast-turnaround implemention of large numbers of integrated system designs (an initial feasibility test was made last year in support of the fall '78 MIT course).

Maskmaking for MPC79 will be done by Micro Mask, Inc., Sunnyvale, CA, using an ETEC electron-beam maskmaking system.

Wafer fabrication for MPC79 will be done by Hewlett-Packard at the HP Deer Creek Research Laboratory, Palo Alto, CA, using an nMOS, depletion-load, silicon-gate process.

Packaging: Wafers will be diced at PARC. The chips will be returned to the universities for mounting and custom wire-bonding (we'll send more info about packaging in later messages). Some schools have inadequate wire-bonding facilities, and a limited amount of wire-bonding may possibly be provided by PARC for those schools; we'd like to hear from other schools or firms that could help provide this wire-bonding support.

3. DESIGN FILE FORMAT; PROCESS; DESIGN RULES;
VALUE OF LAMBDA:

DESIGN FILE FORMAT: CIF2.0, as documented in "Introduction to VLSI Systems", by Mead & Conway, Chapter 4; PROCESS: nMOS, depletion-load, silicon-gate process; DESIGN RULES: Mead & Conway (see Ch. 2 and Color Plates 3 and 4 in "Introduction to VLSI Systems"); LAMBDA = 2.5 microns.

4. AVERAGE SPACE PER PROJECT:

Here are some very preliminary estimates: The total number of projects will be ~ 60 to 100. We are planning to produce two E-beam mask sets, with each mask set containing five to seven different multiproject chip types, with each chip being ~ 6mm by 6mm. Thus, the average student project should be ~ 2mm by 2mm. If a university class wants to send some very big projects, they should plan to compensate by sending some small ones to keep the average size down. [We will soon provide a library of cells, including input and output pads that have a pitch of ~106 lambda. Thus at lambda = 2.5 microns, even a 2mm by 2mm project can have ~7 pads on a side, and can contain quite a lot of stuff.]

We are very interested in supporting serious university research projects with these MPC efforts (such as the recent LISP machine chip designed by Sussman, Holloway, Bell, and Steele). Separate consideration for space allocation will be given for such projects.

5. SOME KEY DATES (these are firm deadlines):

(i) Each school should confirm, by no later than 13 November, that the actual software and hardware to be used for final design file transmission to MAXC is operating correctly. This should be done by placing the CIF design file of a typical moderate-sized design on MAXC (the design doesn't need to be in finished form, and doesn't need to be one intended for MPC79, but it should contain a representative collection of CIF primitives and symbols for the purpose of testing the overall system), and then mailing a checkplot of the same file to Lynn Conway, Xerox PARC, 3333 Coyote Hill Road, Palo Alto, CA 94304. We will plot the file here and compare plots to see if the transmission was successful, the CIF code was valid, etc.

(ii) Preliminary "final" versions of all projects must be submitted no later than 27 November. The final space allocation will be made at this time, with those designs earliest to reach the appearance of final form receiving the highest priority. There will be one week remaining to check for errors and resubmit corrected versions before the design cutoff date. However, dimensions of projects may not increase after this time without risk of losing their space allocation.

(iii) The design cutoff date/time will be 4 December at 5:00pm PST. All accepted projects will be gathered at that time and merged into the mask specifications.

6. SOME THINGS TO DO:

(i) Each school should designate some person(s) to be the project coordinator(s). The coordinator

will relay the MPC79 message information, "rules of the game", etc. to those doing design projects at their school, will interact with MPC79 to set-up and test the file-transmissions procedure from their school, and later-on will interact with MPC79 via messages and file transfers to submit design files for inclusion in the chip-set.

(ii) A MAXC account < universityname-VLSI > has been established at PARC for each of the major participating universities to use for MPC79 design file transfers. The project lab coordinator(s) at each university should select a new password for their university's MAXC account, and notify us of that password (we will put it into effect immediately upon receipt). Also, please message the names of the coordinators, and the names of those who will know the MAXC password.

(iii) We will soon begin to make a gross allocation of space between the various schools, so as to provide you all with better estimates of available space. Later-on we'll make firm space allocations to individual projects, with preference given to those projects that are earliest to reach a near-finished form. Coordinators should keep MPC79 updated on the number of projects likely to be submitted by their university. If a school plans to submit several very large designs, let us know as soon as possible, with estimates of the project sizes. If a school expects to submit fewer designs than the estimates listed in item 1 above, please let us know (we can then make the space available to additional participants).

7. THINGS TO WATCH FOR IN COMING MESSAGES:

Message#2 (~ OCT 17): A small library of useful cells and the procedures for obtaining the library design files will be described.

Message#3 (~ OCT 22): The Request-Acknowledge form of interactions will be described for placing design files for checking and for submitting/resubmitting design files for merging into MPC79.

We welcome the students in the courses to the new and rapidly growing community of integrated system designers and researchers. There's a lot virgin territory for you to explore where few have worked before - it's very likely that some of you will discover important new architectural techniques or gain insight into important new research problems while working on your first design projects. We look forward to the excitement of the final month of project activity later this fall. If you have any questions, send us a message.

The MPC79 Organizers,

Lynn Conway, Alan Bell, Martin Newell, Dick Lyon
LSI Systems Area, Xerox PARC
12 October 1979

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
October 17, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #2**

Filed on: [MAXC]<Conway>MPC79.memo2

This is MPC79 message #2, the official release announcement and documentation of the file of library symbol designs provided for use in the multiuniversity multiproject chip set.

SUMMARY

A single file in CIF 2.0 format is provided for your use. It contains standard I/O Pads, all the pieces needed to make PLA's, shift register cells on a pitch compatible with the PLA, and superbuffers for driving clock and control lines. The intention is that these should be a sufficient set of cell designs to allow implementation of combinational functions and state machines simply by placement and interconnection, thus allowing students to focus their efforts on the architecture, logic, and cell designs specific to their own projects. They also serve as examples, and can be used to test your CIF plotting software.

Project lab coordinators at each participating school should retrieve the file from [MAXC]<MPC79>LIBRARY79-250.CIF (250 is the value of lambda in CIF units, which is 2.5 microns). Additional hardcopy documentation with color checkplots will be mailed later to each school.

CONVENTIONS

Since the library symbols were designed using ICARUS, they all have names in addition to numbers. Names are represented in the CIF file by the use of a userExtensionCommand, in the format "9 name;". These names may be used or ignored, but in this message all symbols are referred to by name. The terms symbol and cell are used interchangeably in this message.

In all cases, the origin of a symbol is the upper left corner of its minimum bounding box; hence, all Y coordinates in the CIF library symbol definitions are negative.

Since this library is intended to be compatible with even the simplest design systems, no geometric primitives other than boxes with default direction and no rotation transformations except multiples of 90 degrees are used; all box edges before and after transformation lie on the lambda grid.

Plots of various symbols should be made from the CIF file to serve as the illustrations for this document.

PAD DESCRIPTIONS

Bonding pads and associated circuitry are provided for input, output, clocked output, tristate input/output, Vdd, ground, and conversion of a single-phase clock input to two-phase.

A standard configuration was chosen to simplify placement and interconnection of the pads. See PadBlank, which is called by most of the other pads, as an example:

```
DS 2;          9 PadBlank;
( 4 Items. ); (bounding box 0, 0 to 26500, -26500);
L NM; B L 26500 W 2000 C 13250,-1000; (Vdd line);
L NM; B L 20500 W 2000 C 13250,-25500; (ground line);
L NM; B L 13500 W 13500 C 13250,-13250; (metal pad);
L NG; B L 11500 W 11500 C 13250,-13250; (overglass window);
DF;
```

PadBlank illustrates the fact that each pad is a 135 micron metal square with a 115 micron square overglassing window in a 265 micron (106 lambda) square area, with horizontal metal lines along the top and bottom edges. The top metal line, which is always used for a Vdd connection, crosses the entire width of the symbol, and defines the outside edge of the project of which the symbol is a part. The default orientation is correct for pads along the top edge of a project. The bottom metal line is used for ground, and stops short of the edges of the symbol to facilitate running Vdd around the corners of a project without going outside the bounding box of the pad symbols. A typical project will have abutting pads around two, three, or four sides, with an 8-lambda Vdd ring around the outside, and an 8-lambda ground ring around the inside; pads should only be placed around the perimeter of a project, since interior pads are difficult to bond. The Vdd pad omits the ground line so that there will be a gap in the ground ring to bring power into the project. See PadSample for an example of all the pads and their power connections.

The pads and their sizes (in lambda) are as follows:

PadBlank	106x106
PadGround	106x106
PadVdd	106x80
PadIn	106x106
PadDriver	106x106
PadOut	106x145
PadClockedOut	106x145
PadTriState	106x170
PadClockBar	106x179

The output pads call PadDriver, which uses enhancement-mode pullups, so the output levels are TTL-like; internally these pads should be driven from level-restored signals. The input pad does no level restoration (it simply provides a lightning arrestor), so inputs from TTL-like devices should connect only to k=8 logic, and should not control pass transistors.

Note that PadClockBar generates inverse clocks, guaranteed to never both be low at the same time, from a single-phase TTL-compatible input; these are driven by a powerful superbuffer for distribution around a chip, and are intended to be used with InvertingSB (described below) to generate clocks and gated control signals. Designers should carefully consider the implications of using this clock generation circuit before including it in their projects; it results in considerably less clocking flexibility than using separate input pads for the clock phases.

PLA DESCRIPTIONS

The PLA symbols provided for MPC79 were designed to be simple and clean, and are not as small as they could be in some cases. The pitch of the metal and poly lines in both planes is 8 lambda, when 7 lambda would be possible. This extra spacing makes layout of the edge cells on the same pitch much easier, and makes possible the layout of a shift register cell on the same pitch as the

PLA inputs (16 lambda). The overall structure and orientation of the PLA is similar to that shown in Mead&Conway's Introduction to VLSI Systems, pp. 102-107 (inputs and outputs on the bottom edge, AND-plane on the left, OR-plane on the right); but, as can be seen by comparing the layouts, the extra spacing simplifies most of the cells.

See PLA-4-8-8 (a 4-input, 8-product term, 8-output PLA) as an example of how the pieces fit together. This layout illustrates the use of extra metal ground meshing that may be needed in large PLA's; typically a ground line for every 32 product term lines will be adequate, but a conservative designer might use more frequent ground lines. This layout also illustrates all the possible clocked and unclocked input and output cells, and the NOR ouput cells (which, if used in place of the usual inverters, effectively AND pairs of adjacent OR-plane outputs to facilitate "folding" of ROMs). For simplicity, no provision is made for an odd number of lines across either plane in either direction.

The basic cells provided are the following (cells marked with * should be rotated 90 degrees clockwise for use in the OR-plane):

PlaCell*
PlaGround*
PlaPullups*
PlaConnect
PlaIn
PlaClockedIn
PlaOut
PlaClockedOut
PlaNorOut
PlaClockedNorOut
PlaHoleWires

These are the programming cells for the left and right sides of the AND-plane cells and the top and bottom of the OR-plane cells:

PlaProgLeft
PlaProgRight
PlaProgTop
PlaProgBottom

In addition, cells are provided to fill the spaces left to accomodate the optional extra ground meshing:

PlaOrSpace
PlaConnectSpace
PlaGroundSpace*
PlaPullupSpace*
PlaOutSpace

SUPERBUFFER DESCRIPTIONS

A set of superbuffers is provided for use as clock and control line drivers. They were optimized for flexibility and regularity, rather than absolute speed. SuperBuffer is a subcell of both InvertingSB and NoninvertingSB, and has no output structure of its own. With alternate cells mirrored, superbuffers fit together with their diffusion outputs regularly spaced 16 lambda apart along the top edge. To simplify placement, mirrored pairs are provided for both inverting and noninverting types.

The symbol SBExample illustrates the use of superbuffers with various input options. Generally, it

is intended that Phi1inverse and Phi2inverse from PadClockBar would be distributed on the metal lines that (partially) cross the bottom edge of the superbuffers, and that clock gating signals would be routed in poly from below (low-true logic) into InvertingSB, making it into a NOR driver. Thus both gated and nongated clocks are driven through the same circuit, with similar delay (but use caution in loading these signals, since fatal clock skew is still possible).

The symbol names are as follows:

SuperBuffer
InvertingSB
InvertingSBPair
NoninvertingSB
NoninvertingSBPair
SBExample

SHIFT REGISTER DESCRIPTIONS

These full-bit shift register cells fit together with a pitch of 16 lambda, which make them useful for serial-to-parallel conversion (ShiftCell) on the pitch of PlaIn or PlaClockedIn, or for parallel-to-serial conversion (PSCell) on the pitch of PlaNorOut or PlaClockedNorOut. These cells have vertical metal power and clock lines, parallel to the direction of shift; they should be rotated to interface with the PLA in standard orientation.

The shift register symbol names are as follows:

ShiftCell
PSCell

CHECKING

It is recommended that each designer take the time to examine library cells in detail before using them, to avoid misuse and to look for possible errors or incompatibilities. Although we have checked the cells carefully, they are not guaranteed to be free of logic, circuit, or design rule errors; if any errors are found, please notify MPC79@PARC immediately (the first person to report each fatal error will be amply rewarded). If anyone documents the cells in more detail, such as coordinates of connection points, etc., we would be glad to collect and distribute that information.

It would be useful if instructors would assign homework problems based on the library, such as to look for errors, to analyze the output pad or the clock pad, to develop formulas for the size and speed of the PLA, to analyze capacitive coupling of the clock to the storage node in ShiftCell, or to look at current limits of the power lines in various cells. We would be glad to see the results of such assignments.

Dick Lyon
17 October 1979

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
November 1, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #3**

Filed on: [MAXC]<Conway>MPC79.memo3

This is MPC79 informational message #3, which describes the procedures that project-lab coordinators should use to submit student design files for inclusion in MPC79 and to check the status of submitted designs. We hope the information and examples in this message are sufficient to serve as a "system user's guide" for the coordinators (sorry the msg is so long, but a bunch of examples are included for completeness; future info msgs will be much shorter).

1. OVERVIEW

MPC79 is being used to test some ideas, operational procedures, and prototype software which simulate an automated "VLSI IMPLEMENTATION SYSTEM". Such systems might in the future reside as servers on the ARPAnet or other networks, queuing up requests for implementation of VLSI designs, packing designs into mask sets, generating a mask specification file when a mask set is fully packed, coordinating and tracking the later mask-fab-packaging steps, routing the packaged chips and associated information back to the designers, and then billing the appropriate accounts.

Designer's interactions with such servers could be kept very simple, being analogous to sending electronically created documents to be hardcopied on a centralized printing server in a computer network: when the document (design) is complete, one merely ships the file to the printer (implementation system) and issues the command HARDCOPY (IMPLEMENT); if the document (design) sits in the printer's (implementation system's)input queue for a while, and an error is found in the meantime, one might issue a command to replace the queued entry with a revised entry, etc.

Due to some practical constraints (number of MAXC accounts, security, etc.), we aren't set up to provide all individual designers direct interactions with the MPC79 system. Instead, most designers at each school will have their interactions handled for them by their project-lab coordinators.

Thus the coordinators carry a heavy responsibility for tracking the progress of the student projects, for promptly sending design files and commands to MPC79 as projects near completion, and for keeping the students informed of the status of their designs in MPC79.

However, coordinator interactions with MPC79 should be simple and straightforward, using very simple requests for service via very concise messages; the messages will be easily constructed in response to the usual message system prompting. At most schools, coordinators will simply send a batch of requests every few days, and check on the status of these requests every few days, mainly during the final weeks before the deadlines. We suggest that each coordinator keep in close touch with their student designers via the electronic message system on the computing facilities used for design support at their school.

Here at PARC the MPC79 organizers will initiate responses to coordinator messages, and will

service the requests in those messages, by simply filling in or moving around text entries in "electronic forms" displayed on our ALTOs. In some cases, the message responses and command actions will be automated, but most will require manual keyboard-display interactions on our part. We now expect to receive and process about 60 to 100 projects from about 8 to 10 different schools; thus the need for simple interactions by formal messages.

The following sections describe the types of requests, and give examples to clarify the request message formats and the effects of request servicing by the system.

Some basic ideas and terms used in the following sections are: (i) each project will be given a unique name (ID); (ii) there are only a few request types, encoded by KEYWORDs; (iii) most requests for service need be only one line of text within a message from the coordinator to MPC79@PARC-MAXC of the form: "KEYWORD: ID"; (iv) when the MPC79 system notices and services a request, it will send a message back to the coordinator, indicating a positive (ACK) or negative (NACK) acknowledgement to that request; (v) as nearly-completed designs having valid CIF code and of acceptable sizes are submitted for implementation and ACKed, they will be entered into a PROJECT PENDING QUEUE (PPQ)in order of date/time first ACKed; (vi) space will be firmly allocated to projects in the PPQ in order of entry; (vii) under certain conditions, projects in the PPQ may lose their ACK status - they must regain it by the cutoff date in order to get into MPC79; (viii) a STATUS FILE will be maintained for each school on MAXC showing the current status of that schools projects.

NOTE: Coordinators should keep their MAXC accounts as free as possible of unused files, to avoid excessive use of MAXC file space and to avoid confusion. Think of MAXC as a temporary place for files in transit into MPC79, rather than as a file repository. Just to be safe, we will periodically run a program (DELVER) that deletes old versions of files from the university-VLSI directories, so that only the two most recent versions of any file are retained.

2. THE TYPES OF REQUESTS:

There are five types of requests for service by the MPC79 system that can be made by the university project-lab coordinators: (a) OPEN a project ID; (b) request that an ID's design file be CHECKed; (c) request that an ID's design file be IMPLEMENTed; (d) DELETE a project ID; (e) message an informal QUESTION/COMMENT/ANSWER about a project.

(a) An OPEN causes the MPC79 system to generate a unique ID for a project, and provides the system information for use when responding to messages related to that ID. The OPEN also conveys a brief project description and estimate of project size - this information will be used for setting a preliminary space division in MPC79 among the various universities. (Note: All lengths used for physical space allocation purposes in MPC79 will be given in physical units of microns, rather than in relative units of Lambdas). Once a project is "OPENed", it will be listed in the STATUS FILE. We will begin processing OPENs starting 8 Nov 79. Schools should supply OPENs for projects ASAP after 8 Nov, in order to get an appropriate piece of the available space.

(b) A CHECK request causes a project's design file to be processed by all MPC79 software up to but not including placement in the Project Pending Queue. A project needn't have had space allocated to it to be CHECKed. A CHECK will determine if a project design file was successfully transmitted to MPC79, and confirm that the project's CIF code is OK (to the extent of the MPC79 checking at that time). Requests for CHECKing may occur before a design is ready for IMPLEMENTation. We will begin processing CHECKs on 8 Nov 79. Remember the deadline: each school or other location must have placed a sample CIF design file on MAXC and mailed us a plot of that design by 13 Nov, so we can test the connection to that location. Use a CHECK request for this purpose; the ID can later be closed if the design isn't to be IMPLEMENTed.

(c) An IMPLEMENT request causes a project's design file to be processed by all MPC79 software, to be placed into the Project Pending Queue (if its CIF code is OK), and then to be given a FIRM Bounding Box Space Allocation (if space is available) for merging and implementation in MPC79. Even if the IMPLEMENT is successfully ACKed, the project designer should continue to look for errors (logic, design rule, etc.) in the design. If any are found, they should be fixed; the design file should then be replaced on MAXC, and another IMPLEMENT request issued; this may be done without risk of loss of the design's space allocation, so long as its Bounding Box doesn't increase in size. If the Bounding Box grows, the IMPLEMENT will probably be NACKed, especially late in the game as space is running out. If an IMPLEMENT is NACKed, the designer should be notified by the coordinator ASAP, so that another IMPLEMENT can be attempted. We will begin processing IMPLEMENT requests on 16 Nov 79.

(d) The DELETE request enables removal of an ID from the system by deleting all information from the system related to that ID. Some reasons for a DELETE: A student gets sick, and can't complete their design; a major error in a design is discovered too late to be fixed; the coordinator at a school may want to reallocate space from one big design to several small ones, or vice-versa.

(e) Since the system we're using to conduct MPC79 is an incompletely automated prototype system, and since there's a lot of new and incompletely tested software both here and in the universities, we need an "out" to cover contingencies, disasters, confusions, coordinator or organizer collapse, etc. So, coordinators may request an answer to a QUESTION or send us a COMMENT concerning an ID. We'll ACK these in the usual way (when we're able to get around to them). Similarly, WE may initiate a QUESTION/COMMENT/ANSWER interaction with a project coordinator. However, let's all try to keep this kind of informal interaction to a minimum, and see how far we can get with simple OPEN, CHECK, IMPLEMENT, and DELETE requests.

NOTE: By mid-November we'll process pending requests once every day or two, more frequently as the deadlines draw near. It's possible that multiple requests might be sent regarding one ID before any ACK/NACK is returned by MPC79. In such cases MPC79 will service ONLY the most recent request against the latest file version for that ID.

NOTE: We aren't able to provide users with a "full service". For example, there is no request type "CHECKPLOT" - - -

3. DETAILED DESCRIPTIONS & EXAMPLES OF REQUESTS

NOTE: Please identify requests using keywords followed by colons, as shown below. (In the following, some names & places are real. However, the events are fictitious!).

(a) OPEN:

To OPEN a project ID, the coordinator should send to MPC79@PARC-MAXC a message containing (i) a list of the fullname(s) of the designers of the project, (ii) the person(s) to whom we should send ACKs (usually the coordinator(s)), (iii) persons to copy on the ACKs (perhaps the designers if they have ARPANET mailboxes), (iv) a brief informal description of proposed project (a couple of sentences will do), and (v) a rough estimate of project size (Bounding Box,in microns, for space allocation purposes). Multiple ID OPENs may be requested in a single message; if this is done insert blank lines between the OPENs.

Example of an OPEN request:

- -

Date: 16 Nov 1979 at 0930 EST
To: MPC79@PARC-MAXC
From: REB@MIT-XX
Cc: REB@MIT-XX
Subject: REQUEST

OPEN:
Designer(s): Jim Smith, Jack Jones
ACKs to: REB@MIT-XX
Copies to: SMITH@MIT-AI
Description: This project is a 4-bit slice of an ALU
Est.BB: ~ 1600 X 2600 microns.

OPEN:
Designer(s): Bill White
ACKs to: REB@MIT-XX
Description: Project is a Writeable PLA
Est.BB: ~ 1800 X 2400 microns.

- -

On receiving an OPEN Request, the MPC79 system will (i) establish a "project ID", (ii) file the OPEN information for use when responding to further Requests, (iii) establish and maintain an entry for that ID in the STATUS FILE, and (iv) either Acknowledge the Request by returning the value of the project ID, or Negative Acknowledge the Request with a reason (for example, late in the game we may stop opening ID's). All OPEN REQs will be individually ACKed/NACKed.

Example of an OPEN Acknowledgement:

- -

Date: 16 Nov 1979 at 1820 PST
To: REB@MIT-XX
From: MPC79@PARC-MAXC
Cc: SMITH@MIT-AI
Subject: ACK to OPEN: 16 Nov 1979 at 0930 EST.

Design by Jim Smith, Jack Jones given project ID: SmiJonMIT

- -

(b) CHECK:

To CHECK a design file, the coordinator should (i) place the design file on [MAXC]<universityname-VLSI> using the filename ID.CIF, where ID is the value returned by MPC79 in the ACK to the OPEN for that project, and then (ii) send a message to MPC79@PARC-MAXC requesting "CHECK: ID", as illustrated in the following example. A project needn't have obtained space allocation in MPC79 in order to be CHECKed. For example, the design could be in preliminary form, and be entered for CHECKing in order to test the overall communication link from the university to the MPC79 system, or to test the compatibility of CIF software at both the university and the MPC79 system. Multiple CHECKS may be requested in one message; if this is done, insert blank lines between CHECKs.

Example of a CHECK Request:

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- - - - - - - - - - - - - - - - - - - - - -
Date: 19 Nov 1979 at 1044 PST
To: MPC79@PARC-MAXC
From: ICL.ISL-ROB@SU-SCORE
Cc: ICL.ISL-ROB@SU-SCORE, ICL.ISL-NUKE@SU-SCORE
Subject: REQUEST

CHECK: RobMSU

CHECK: AndyBSU
- - - - - - - - - - - - - - - - - - - - - -
```

On receiving a CHECK Request, the MPC79 system will pass the design file ID.CIF through all stages of processing up to but not including insertion into the Project Pending Queue, and will either (i) send back an ACK for that ID, which indicates that no errors in the CIF code occurred, or (ii) send back a NACK, indicating an error, along with a brief text comment describing the error. All CHECK REQs will be individually ACKed/NACKed. The time of the CIF file's placement on MAXC and the project's Bounding Box size will be included in the ACK/NACK message.

Example of a NACK to a CHECK Request:

```
- - - - - - - - - - - - - - - - - - - - - -
Date: 20 Nov 1979 at 2018 PST
To: ICL.ISL-ROB@SU-SCORE
From: MPC79@PARC-MAXC
Cc: ICL.ISL-NUKE@SU-SCORE
Subject: NACK to CHECK:RobMSU

NACK to CHECK [MAXC]<SU-VLSI>RobMSU.CIF;1 created 1021/11-19-79.
BB 2200x3200 um.
CIF error: no END statement (did the whole file get to MAXC?)
- - - - - - - - - - - - - - - - - - - - - -
```

(c) IMPLEMENT:

To submit a design file for IMPLEMENTation, the coordinator should (i) place the design file on [MAXC]<universityname-VLSI> using the filename ID.CIF (where ID is the value returned by the MPC79 system in the ACK to the OPEN for that project), and then (ii) send a message to MPC79@PARC-MAXC requesting "IMPLEMENT: ID", as illustrated in the following example. Multiple CHECKs and IMPLEMENTs may be requested in a single message; if this is done, insert blank lines between requests.

Example of an IMPLEMENT Request:

```
- - - - - - - - - - - - - - - - - - - - - -
Date: 23 Nov 1979 at 1845 PST
To: MPC79@PARC-MAXC
From: ICL.ISL-ROB@SU-SCORE
Cc: ICL.ISL-ROB@SU-SCORE, ICL.ISL-NUKE@SU-SCORE
Subject: REQUEST

IMPLEMENT: RobMSU
- - - - - - - - - - - - - - - - - - - - - -
```

On receiving an IMPLEMENT request, the MPC79 system passes the design file ID.CIF through all stages of processing for CHECKing, inserts the design into the Project Pending Queue (if the CIF code is OK) and then allocates space (if space is available). It then either (i) sends back an ACK for that ID, which indicates that no errors in the CIF code occurred AND that space was allocated, or (ii) sends back a NACK along with a brief text comment describing the error or space allocation problem. All IMPLEMENT requests will be individually ACKed/NACKed, with the CIF file's time stamp of placement on MAXC and the BB size included in the message.

Example of an ACK to an IMPLEMENT request:

- -

Date: 24 Nov 1979 at 0700 PST
To: ICL.ISL-ROB@SU-SCORE
From: MPC79@PARC-MAXC
Cc: ICL.ISL-NUKE@SU-SCORE
Subject: ACK to IMPLEMENT:RobMSU

ACK to IMPLEMENT [MAXC]<SU-VLSI>RobMSU.CIF;4 created 1800/11-23-79.
BB 2200x3200 um. Space Allocated.

- -

Example of a NACK to a IMPLEMENT request:

- -

Date: 26 Nov 1979 at 0700 PST
To: ICL.ISL-ROB@SU-SCORE
From: MPC79@PARC-MAXC
Cc: ICL.ISL-NUKE@SU-SCORE
Subject: NACK to IMPLEMENT:RobMSU

NACK to IMPLEMENT [MAXC]<SU-VLSI>RobMSU.CIF;6 created 1340/11-25-79.
CHECKs OK.
BB 2400x3200 um.
BB has grown from previous Allocated BB of 2200x3200 um.
Space not available. Resubmit to Allocated size.

- -

NOTE: We'll be taking a closer look at designs during the final week before 4 DEC, when they are supposedly in near-final form. It is possible that an IMPLEMENT request may receive an ACK from the MPC79 system, and then at a later time our further checking (for example plotting) reveals a fatal error in that design (for example, incorrect layer names throughout a design, gross design rule violations, etc.). If this occurs, the MPC79 system may generate a "Delayed NACK" of that design. So, although the design has achieved a space allocation, it can lose its ACK status at any time, and we reserve the right to do this. The designer must then update the design and the coordinator issue another IMPLEMENT request to try to regain ACK status for the design. The NACK must be replaced by an ACK before the design cutoff date (see item 4).

Example of a Delayed NACK to an IMPLEMENT Request:

- -

Date: 29 Nov 1979 at 2250 PST
To: FOSTER@CMUA
From: MPC79@PARC-MAXC
Cc: HT.KUNG@CMUA
Subject: NACK to IMPLEMENT:MFHTCMU

NACK to IMPLEMENT [MAXC]<CMU-VLSI>MFHTCMU.CIF;3 created 0700/11-25-79.
BB 2800x3000 um. Space Allocated.

Found a fatal error when plotting. Should be easy to fix.
VDD and GND short near logo. Please fix and reissue IMPLEMENT ASAP.
- -

(d) DELETE:

To DELETE an ID, simply send a REQUEST message containing DELETE: followed by the ID. The DELETE will cause deletion of all information related to that ID from the MPC79 system, and will be ACKed by the system when completed. If the reason for the DELETE is a decision to reallocate space to other projects that are on the Project Pending Queue, give the details in the message.

(e) QUESTIONS/COMMENTS/ANSWERS:

If it should become necessary to send a QUESTION or COMMENT, or to ACKnowledge a QUESTION from MPC79 with an ANSWER, use informal messages formatted somewhat like the above.

Example of a QUESTION Request:
- -
Date: 30 Nov 1979 at 1225 CST
To: MPC79@PARC-MAXC
From: FOSTER@CMUA
Cc: HT.KUNG@CMUA
Subject: REQUEST

QUESTION: MFHTCMU: Can't find the error mentioned in your NACK of 29 Nov at 2250.
Have you got a problem with your plotting software?
- -

3. READING THE STATUS OF THE PROJECTS

A file will be maintained for each university on the MPC79 account on MAXC containing the STATUS of that university's projects.

These files will be named [MAXC]<MPC79>universityname.STATUS, where
universityname = "MIT"|"CMU"|"UOFR"|"SU"|"CALTECH"|"UCLA"|"OTHERS".

The project coordinators can read or retrieve these files at any time. For each project ID, the file will contain: the designer name(s); BB in um; AREA in square mm's; if in ACK or NACK STATUS; if project is in the Project Pending Queue; if SPACE is ALLOCATED; the time/date of latest file creation; the time/date of first ACKed IMPLEMENT(sets priority); comments in unformatted text including project decription, open questions, reason for a NACK status, etc.

We suggest that the coordinators retrieve, hardcopy, and post the STATUS file from time-to-time, especially during the final weeks of MPC79, so that students can follow the action.

4. THE COMING SPACE WAR

The above message suggests the space allocation algorithm we'll be using: Basically, it is first-come first-served. While the service is free, participation is somewhat competitive. The PRELIMINARY space partitioning among schools will depend on early OPENs of interesting-sounding projects. (We may modify this partitioning later-on as events unfold). The actual FIRM space allocations among individuals (and the positions in the Project Pending Queue of designs without space allocation) will be prioritized by the first ACKed IMPLEMENT DATEs/TIMEs of individual designs in near final form.

Preliminary final versions of designs (i.e., valid CIF, BB firmly fixed and not to grow, appearance of nearly completed design if plotted) must have been placed by 27 November. Some of these designs may receive space allocations prior to the 27th, but on the 27th we will attempt to make a complete allocation, so that students will know whether or not they are certain to get in the chip set if they finish their designs.

On the design cutoff (5:00pm PST, 4 Dec), all projects having firm space allocation and ACK status will be merged into MPC79; those with firm allocations but in NACK status will be deleted; any remaining space will then be allocated to ACKed projects in the Project Pending Queue, in priority order. We'll send out more messages about space allocation later on as designs are filed on MAXC and we begin to get a feeling for the actual demand vs available space.

Lynn Conway and Alan Bell
LSI Systems Area, Systems Science Laboratory, Xerox PARC
1 November 1979

- -

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
November 6, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #4**

Filed on [MAXC]KConway>MPC79.memo4

This is MPC79 informational message #4, which describes some of the conventions in use for interpreting CIF files. The principal reason for this message is to define the MPC79 interpretation of those aspects of CIF that are influenced by implementation considerations and which typically vary from installation to installation as a function of the plotting and patterning devices to be used.

As was mentioned in Message #1, full CIF 2.0 (as documented in Chapter 4 of "Introduction to VLSI Systems" by Mead and Conway) is being supported by MPC79. Many of the subtle CIF implementation considerations are discussed in Chapter 7 of the upcoming Second Edition of "A Guide to LSI Implementation" by Hon and Sequin (an advance copy of this chapter has been sent to all project coordinators). An overview of some of the more relevant issues is given in this message.

A further motivation for this message is that we can provide better support if certain restrictions are observed. Furthermore, certain constructs take much more processing time than others and we would like you to be aware of these considerations.

1. CIF CONSTRUCTS

This section presents our interpretation of certain CIF constructs.

Box: Straightforward interpretation.

Roundflash: Approximated by an octagon that is always aligned with the overall chip axes.

Wire: For wire segments involving turn angles up to and including 90 degrees the interpretation used is exactly that suggested in Ch. 7 of the Implementation Guide. For sharper angles, no "extension" of the segments is used, but a Roundflash is output at the corner. The ends of wires are always squared off. This interpretation does lead to a sudden change in the shape of a corner as the corner angle passes through 90 degrees, but it was chosen to allow efficient processing of the common case of wires consisting of segments aligned with coordinate axes.

Polygon: All variants of polygons are supported, including non-convex and those with a self intersecting boundary. A point is considered to be inside the polygon if the winding number of the boundary with respect to that point is non-zero. That is, for a point to be considered inside the polygon, a line joining the point to a point moving along the boundary must make a non-zero net number of complete rotations around the given point as the boundary point makes one traversal of the boundary. This interpretation was motivated by the desire for the same results when a self intersecting wire is represented as a CIF wire or as a CIF polygon describing the boundary of the wire. This interpretation is described more fully in Ch. 7 of the Implementation Guide.

User Extension Command: All user extension commands are treated as comments, except that a warning is given.

Layer Names: The following six mask layer names will be recognized and will lead to the inclusion of the affected geometric items into the indicated MEBES mask layer file:

ND Diffusion
NP Polysilicon
NC Contact cut
NM Metal
NI depletion mode Implant
NG overGlass opening

Anything defined on a layer of any other name is treated as unknown, is ignored, and a warning is given. For example, layer NB (Buried contact) is treated as unknown since buried contacts are not supported by MPC79. Layer NX (which is used once in the library sent out) is also in this category.

In general we do not request that the fabrication facility overglass wafers containing multiproject chips. However, overglass masks will be produced for MPC79, and it's possible that some fraction of the MPC79 wafers will be overglassed. Therefore, any bonding or contact pads should have appropriate cuts specified in the overglass layer of the project's CIF file. The Pads in the MPC79 library have such cuts specified, so it will be necessary to specify overglass cuts only if you use some other bonding pads or if you intend to use probe pads.

Delete Definitions (DD): Interpreted as in Ch. 7 of the Implementation Guide. Note that we do not require any DD commands between project files, since in the MPC79 effort we are requiring that projects be self-contained (see also item 3.), so that we can independently process and merge projects into the starting frames.

Warning messages: Our CIF parser produces warning messages on detecting certain questionable constructs (such as zero-width wires, among other things). These may or may not result in the design being NACKed, depending on whether it appears that the error is in fact fatal or not. However, even if the design is ACKed by us, any warning messages should be examined carefully to see if they indicate some serious error.

2. CONSEQUENCES

Roundflash and Wire: In view of the variation in interpretation from installation to installation of the circular arcs found in ideal wires and flashes, it is advisable to adopt a conservative approach to the use of wires. Two extreme approximations to the ideal shapes can be considered - inscribing and circumscribing. If you wish to ensure contact between a wire or flash and some other object in your design (independent of the implementation system to be used) then you should make certain that a system using an inscribing approximation would still place these objects in contact. To ensure adequate separation between a wire or flash and some other object (independent of the implementation system to be used) make certain that a system using a circumscribing approximation would still position these objects with sufficient separation. Whenever the need arises for more precise control over the geometry than can be realized by the above approach then do not use wires or flashes, but use boxes or polygons instead.

The interpretation of Roundflash and Wire commands in MPC79 gives a circumscribing approximation. Consequently there should never be any problem with relying on one of these constructs touching another if that is what is desired. However, design rules may be encroached

upon in some cases where use of the ideal shapes would cause no problems. In particular, consider the corners of the squared off ends of wires, and 90 degree bends.

Polygons: The interpretation of polygons differs from the convention sometimes used in computer graphics of considering that a point is inside a polygon if a line drawn from the point to infinity in any direction intersects the boundary an odd number of times. The interpretation used here is believed to be more relevant to the needs of mask layout. If you are using a different convention, and you have polygons with self-intersecting boundaries, then it will be necessary for you to make adjustments.

3. IMPLEMENTATION ISSUES

CIF Libraries: Each CIF file must provide a complete specification of the design, including copies of any library symbols used. Do NOT assume that we will prefix each project with a copy of the library sent to you. For each project it will be necessary for you to extract, from the libraries provided to you, copies of the symbols used by that project, and to include them in the CIF file for the project.

The impact of your choice of a CIF subset: Various subsets of the full CIF 2.0 may be worth considering for a variety of reasons. It should be remembered that the MPC79 system is experimental, and involves the use of much new and unproven software. Consequently you may hurt yourself, and others, if you set out to push all the facilities to the limits in an attempt to thwart the system. Furthermore, the amount of processing involved in MPC79 will require many hours of computing time here at PARC. Features such as arbitrarily rotated symbols, and contorted wires and polygons can greatly expand the processing time required. Indeed, extreme examples of enormous fully instantiated files that make grossly inefficient use of CIF may find themselves NACKed. You would therefore be doing us (and probably yourselves) a favor if you keep it simple wherever possible.

ICARUS: At several schools the Alto-based system ICARUS is available. A subset of CIF can be converted to and from ICARUS format for viewing or modifying on an Alto. If this is likely to be of interest then the CIF file should contain only Boxes that have rotations of integer multiples of 90 degrees, and Wires having segments aligned with the coordinate axes. Symbol rotations must be constrained to integer multiples of 90 degrees also.

Check Plots: While we are not routinely providing a plotting service, we will be making use of check plots to check on certain designs. Errors found while examining these plots will be reported to you if we believe they represent errors on your part. Consequently, it may be in your interest to make plotting easier for us. At the time of writing this message we have two methods for obtaining check plots, (1) by converting to ICARUS and using its facilities for Versatec and color plots, and (2) by direct plotting of the individual layers on the Versatec only. The first of these gives nice plots but imposes the constraints on CIF cited above. The second is driven off our MEBES conversion software and as such implements everything, however the plots are of single layers only. While we hope to achieve the best of both these worlds in time for use during the later stages of merging MPC79, we cannot be sure of this.

Martin Newell, Alan Bell, Dick Lyon, Bob Hon
LSI Systems Area, Systems Science Laboratory, Xerox PARC
6 November 1979

- -

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
November 26, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #5**

Filed on [MAXC]<Conway>MPC79.memo5

This is MPC79 informational message #5, the final general informational message prior to the design cutoff date. This message (1) discusses some issues related to the open "publication" in MPC79 of design layouts, (2) suggests some basic documentation that designers might include as comments within their CIF code, (3) presents some information concerning the starting frame and packaging, and (4) outlines future messages to be sent and a report to be produced concerning MPC79. Project lab coordinators should pass copies of this message on to the participating designers.

1. THE PUBLICATION OF DESIGN LAYOUTS: SOME ISSUES & OPPORTUNITIES:

The capability for teaching VLSI design courses in the universities and then providing students and university researchers with fast-turnaround implementation of design projects is quite new. Such new technological capabilities often raise novel and unpredicted legal and ethical issues. For example, a question that some designers out there may need to think about is what effect (if any) the open publication of the layout of their design may have on possible proprietary interests they or their organization may have in the design.

The implementation of the MPC79 multiproject chip set is being conducted by the implementing organizations on an open and public basis. There is really no alternative for us since we are using a prototype implementation system, and such things as data security (and also accounting, automated scheduling and planning, etc.) are being deferred to future efforts. The "printing" of the wafers containing the MPC79 projects will be much like the open "publication" of a group of technical articles. We ourselves aren't making any particular efforts to legally register or protect any of the information submitted for inclusion. Our major interest in this effort is to further test the feasibility of large-scale, remote-entry, fast-turnaround implementation of VLSI designs.

There are a number of traditional legal mechanisms for protecting novel designs or works of art (e.g. patents, copyrights, trade-secrets). The inclusion of a design in MPC79 doesn't necessarily preclude use of any of these traditional protections. These can be explored by individual designers (and/or their organizations) on a case-by case basis, as needed. However, do note that the inclusion of a project in MPC79 will result in a release into the public domain of a portion of the information associated with that design, and amounts to a limited form of "publication".

The novelty of this implementation effort will probably generate considerable interest. The various artifacts (plots, chips, chip photographs) associated with MPC79 will get a lot of public exposure. Various portions of these will be reproduced in technical reports and journal papers to be authored by some of the participants (both designers and implementers). It is even reasonable to expect that people at the various schools will examine and analyze available information about designs from other schools, in order to assess the differences in results at the different schools. The design files themselves will exist in several computers including those at the originating university. Thus it is

even possible that some design files could be be released into the public domain, as a function of the data security and the policies at the various intermediate sites they pass through.

O.K., that all sounds like some folks might lose a fraction of their potential proprietary interests in their designs if they include them in MPC79. However, there is another way to look at all this. Because of the large audience that will observe the results of MPC79, any marks placed into the layout itself which identify the design and designer will insure that a large peer group knows who did what. Thus, to whatever extent desired, a designer can obtain recognition in the usual form by obtaining "first publication" via this new medium of "publication".

And so, I suggest that designers at least put their name and/or logo, and perhaps a descriptive design title, right in the layout. If fairly large features on the metal level are used for this purpose, the information will show up well in chip photographs. If this is done, then future plagiarism can at least be recognized. Also, someone wanting to use a design would be able to identify, and then contact and negotiate with the original designer.

There are undoubtedly many interesting underlying issues lurking here that members of the technical community might discuss further with colleagues in law schools, business schools, and public policy groups. Perhaps a fundamental question is what legal and cultural traditions would best strike a balance between providing rewards and protection to the creative designer while at the same time stimulating research and innovation through the free exchange of ideas.

2. DOCUMENTATION OF DESIGNS: SOME SUGGESTIONS:

Because of the wide exposure of MPC79 artifacts, there will likely be requests for further information about particular designs or designers. For example, a company may wish to know how to contact the person who designed project X, in order to inquire about their availability for employment or consulting. We plan to list a moderate amount of basic information (such as designer names, schools, organizations, and project titles, as available) in our future technical reports on MPC79.

Those designers who are interested in receiving this sort of exposure should send some basic documentation along with their design files. A good way for designers to send this information is to insert it as CIF comments right at the beginning of their design files. I suggest that designer(s) include their name(s), school and department address, company name and address if they also work in industry, a short abstract describing their design, and pointers to any available or planned documentation or reports concerning the project.

3. STARTING FRAME AND PACKAGING INFORMATION:

The layout of the starting frame for MPC79 has been completed. There will be only one die size: 7696 X 6477 microns (~ 303 X 255 mils). This is the size as measured from scribe line center to scribe line center, prior to sawing up the wafers. The largest metal-line bounding-box that can be contained within the starting frame is 7548 X 5960 microns. The individual die sizes after sawing will be ~303 X 255 mils plus or minus a couple of mils, depending on how each die fractures below the saw cuts around its periphery (sorry about the English units, but the packaging industry still lives in the past and specs everything in mils). We recommend using standard 40 pins packages with cavity sizes of no smaller than 310 by 310 mils. (Use of larger cavity sizes, for example 340 X 340 mils, might be better since wire-bonding the pads near the edges of the chips would be made easier).

We have access to limited packaging capabilities, and a modest supply of 310 X 310 mil cavity 40

pin packages. We'll likely be able to do the packaging and wire-bonding for a few of the smaller isolated design groups that don't have any access to packaging equipment. We'd appreciate hearing from all the project lab coordinators so that we can learn of your school's capabilities and plans (or lack thereof) for doing the packaging of your MPC79 project chips. If you are planning to do your own packaging, you should either have packages in stock or be able to scrounge them from some local company, or else you should order them instantly in order to have them on hand in time when the wafers are ready. If you have access to local industrial help for packaging, and are able to arrange for some of the other schools to have chips packaged, let us know. Especially let us know if you plan to count on us to do your packaging.

The starting frame surrounding every die type will contain several test patterns having pads that can be be probed or wire-bonded that can be used to confirm that the process worked successfully and also to measure performance and certain electrical parameters. Included are four discrete devices (all having channels 5 microns long and 10 microns wide): (i) an enhancement mode FET, (ii) a depletion mode FET, (iii) a metal-gate field-oxide FET, and (iv) a poly-gate field-oxide FET. A ring-oscillator is included that can be used to measure the transit-time of minimum-sized devices. Also included are two Van der Pauw 4-point resistance measuring structures, to enable measurement of the resistances of specific poly and diffusion paths.

4. FUTURE MESSAGES & REPORTS ON MPC79:

Various announcement messages and messages to specific coordinators or designers will be sent out as needed between now and 4 December. Project lab coordinators should watch their mailboxes closely, especially during the final days before the design cutoff. Note: If project coordinators are ever unable to contact MAXC over the net, don't panic, but try again an hour or so later. In the unlikely event that MAXC goes down for more than on hour (especially if some time during the crunch of the last few days before the design cutoff), we will send out advisory messages to all coordinators via other HOST machines on the ARPANET.

After 4 December we will periodically send out status messages to help you track the progress of the maskmaking and wafer fabrication and to help you plan for the arrival of your wafers/chips.

During January and early February we will be seeking information from those participants who have by then tested their projects. We will be accumulating information about the results of the projects at the various schools, and will send out messages sometime in February summarizing this information.

During January and early February we will be documenting the results of MPC79 for inclusion as part of a Xerox PARC/SSL Technical Report by L.Conway, A.Bell, and M.Newell entitled something like "The Implementation of VLSI Systems". This report will likely be available by April '80. (If you'd like to receive a copy of this report, send a msg to Doughty@PARC-MAXC).

Well folks, were now entering the final week before the design cutoff. Good luck on finishing your projects! Watch your electronic mail to find how it all finally turns out.

Lynn Conway
LSI Systems Area, Systems Science Laboratory, Xerox PARC
26 November 1979
- -

Date ?

Well folks, we're nearing the final design cutoff time! We want to congratulate the many project coordinators and designers out there who have managed to keep up with the demanding schedules and deadlines of MPC79. So far we have about 70 designs likely to make it into MPC79.

The available space is fully allocated. A number of projects previously in ACK status with Space Allocation have since increased in size. These will lose their firm Space Allocation, but will remain on the Project Pending Queue, awaiting allocation (most of these will likely make it). We can't be sure how it will finally turn out, since a lot depends on the packing density effectiveness of our planning software, as run on this specific set of projects.

Since there are a number of projects awaiting allocation, it would be a great help if project lab coordinators would notify us ASAP if there are any projects in ACK status that they know will not be finished in time. Such projects should be DELETEd so that others will have a chance to be included. Even if there are no other designs pending from your school, such DELETions may make space available to someone from another school.

We will attempt to group projects together by school onto the different die types. This will make the later distribution of chips, and the distribution of chip-photos, etc., more efficient. One thing for instructors and lab coordinators to consider: If a bunch of your projects are in a visibly unfinished state, they will greatly detract from the effectiveness of your school's chip-photos, etc. We are not looking at plots of all projects to see if they appear completely finished. We guarantee only that the design files will successfully pass through our processing software. (Even if we could plot all the projects, which we can't due to the plotting time involved, there would be difficult questions of interpretation). So, we ask you coordinators to please pass a final filter over your school's designs (perhaps ask to look at a plot of any designs that are late in nearing completion), and Request a DELETE of any that are unfinished.

[A suggestion: It would be a good idea for coordinators to get a list of the names, addresses, and phone numbers of the participating designers, so that you can contact them (probably in early January) when the chips are ready. We will prepare various reports, make up some chips photos, etc., which you or we could also distribute to the participants, if we have all the names and addresses.]

Remember, the deadline is Tuesday, 4 December, at 5:00pm PST. At that time we will stop processing Requests, and will run the Planning, Packing, Merging, and MEBES Conversion software against the collection of projects in ACK status, pulling in as many projects pending allocation as possible.

We would appreciate it if at least one coordinator or instructor from each school would remain available for last-minute questions or decisions. We will be doing quite a bit of plotting once we have merged groups of projects into starting frames. We might, for example, spot what appears to be a fatal flaw in a design at

that point. If we can reach you for information, you can help us make a decision on whether to dump the project or not.

Since these interactions will be few, but must be quite interactive, we suggest that you message us the name and phone number of the coordinator or instructor for your school who could be reached by phone between the hours of 5:00pm and 8:00pm PST (8:00pm and 11:00pm EST) tomorrow. By 8:00pm PST all the hard decisions will have been made.

We will send out a message later this week, summarizing the final status of the MPC79 merging, indicating which designs actually made it into the chip set, etc.

Lynn Conway, Alan Bell, Martin Newell

Reb
Joy
MF40
Doug
Carlo
Izun
Martin
ROB
MUNC
Forest
Bowlf
MPC79
N.hrs
Sur
AB
Conwy

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
January 5, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #6**

Filed on [MAXC]<Conway>MPC79.memo6

The MPC79 implementation has been successfully completed! The chip-set includes 82 VLSI design projects from 124 designers. The implementation turnaround time for MPC79 was 29 days. (from design files to distribution of packaged chips).

Packages containing the project chips were distributed on January 2, 1980. On January 2 the packages were hand delivered to Caltech, Stanford, and U.C.Berkeley, and were mailed special delivery to instructors or coordinators at M.I.T., CMU, Univ. of Rochester, Univ. of Illinois, and the Univ. of Washington. Packages were mailed to individual designers at Univ. of Colorado and Univ. of Bristol the following day. All coordinators should have received the shipments by now. It's likely that most of the chips will be distributed to the student designers during the next few days, just as the new semester begins at most of the schools.

This message (i) provides information about the implementation activities during the past 4 weeks, (ii) describes what the MPC79 shipments contain, and (iii) describes some things that coordinators should do before distributing the chips and their documentation. It also discusses our plans for further documentation concerning MPC79, and our interest in receiving feedback from the designers, to include in that documentation.

If you have any questions or wish to provide testing results or other feedback, you can continue to reach us via MSGs to MPC79@PARC-MAXC.

THE EVENTS SINCE DECEMBER 4:

The events of the past four weeks since the design cutoff time of 5:00pm Tuesday December 4 have been as follows:

We started final processing of the implementation REQUESTs immediately following the design cutoff time. This processing continued on into the evening. During the night of 4-5 December we operated the MPC implementation system to plan and effect the merging of the projects into the various MPC79 chip-types, and to then convert the merged CIF files into MEBES format files. At 10:00 am the next morning we took the merged mask-specification data to Micro Mask.

Delivery of the masks was pipelined with the early fabrication steps, with the first mask of both mask sets being delivered at 5:00 pm, Thursday Dec. 6. By then, HP-ICPL had already started the

processing and were ready for the first masks. Processing continued normally except for one major contingency: the failure of a poly-deposition system (causing a delay of about 8 days for repairs, and leading to an additional delay in wafer processing due to the Christmas holidays). At 10:00 am on Dec. 28, the type-B wafers completed fabrication. The ring oscillator test structures were probed and found to work. One project, Jim Clark's system-clock, was bonded and tested on the afternoon of Dec. 28, and was found to work completely. On Monday Dec. 31 the type-A wafers completed fabrication, and were found to be satisfactory. Packaging, bonding, document generation, and document printing proceeded through January 1. The shipments were mailed at 5:00 pm, January 2.

WHAT THE SHIPMENTS CONTAIN:

The shipment to each university contains (i) a collection of boxed, wire-bonded, packaged chips for that group of designers, (ii) a set of wire-bonding maps for those chips, marked-up to show the custom wire-bonding of each project, (iii) copies of the "MPC79 Implementation Documentation" to be distributed to all designers, and (iv) a questionnaire and return envelope for the designers, so that you all can provide us with some feedback. Coordinators should check to make sure that all this stuff is included in their school's shipment. This shipment provides each project coordinator with ONE packaged, wire-bonded chip for each PROJECT, and ONE set of documentation for each DESIGNER and for each STUDENT in the design course (including those who did not complete a design).

[Some unpackaged chips are also included in certain shipments. These can be packaged by the universities, and used by designers who need a second copy if they suspect that their first copy has manufacturing defects. We'll provide additional unpackaged chips later on. We can provide some additional packaged wire-bonded chips on request (depending on demand and timing); we'll expedite further packaging for those designers who are seriously testing their projects.]

DISTRIBUTING THE CHIPS AND DOCUMENTS:

Coordinators should carefully read Sections 2, 3, and 7 of the "MPC79 Implemention Documentation" before distributing the chips and the documentation to the designers.

Each boxed, packaged chip is marked with a code number. SECTION 2 of the Implementation Documentation describes how to associate these code numbers with the project ID's, so you can figure out which box belongs to which designers(s). SECTION 2 of the documentation also provides important warnings and tips about how to handle the chips and how to prepare them for testing. PLEASE request that designers READ SECTION 2 of the Implementation Documentation before doing anything with their boxed chips.

TESTING:

It is now up to you coordinators and designers to get those projects tested! Be sure to let us know how things went. We'd like to know which projects worked, and which ones didn't. Of the ones

that had bugs, we are very interested in the nature of the bugs, and also whether, and how, you figured out what went wrong. A short one-page questionnaire and a return envelope have been included for each student in the shipments. You can use these to send in your detailed test results. Try to get as many questionnaires back to us as possible before 31 January 1980. You can also send us test results by MSGs to MPC79@PARC-MAXC.

OUR PLANS FOR FURTHER DOCUMENTATION:

We are compiling a proceedings documenting the MPC79 effort, to be published as a Xerox PARC/SSL Report entitled: "Proceedings of the MPC79 Multi-University Multiproject Chip Set Project", edited by A.Bell, L.Conway, R.Lyon, M.Newell. This proceedings will include a general overview of MPC79, photos of various die types, information from the MPC79 ARPANET message traffic, information about the MPC Implementation System, and feedback from the universities.

We hope to include a collection of short-form project reports describing a number of the MPC79 projects (an example of such a report is included in the Implementation Documentation). Coordinators should especially encourage the designers of innovative projects to send us a report for the Proceedings (the deadline for reports is February 29, 1980). Designers may use the MPC79 questionnaires to let us know of their plans to submit a report.

The Proceedings will be printed in large quantities and distributed widely in the universities and in industry. We will send out copies to all participants. Instructors and coordinators: Make sure that your school is represented by some good reports in the Proceedings! For any of you designers who'd like some visibility, now's your chance!

PLANS FOR CHIP PHOTOS:

A commercial photographer will soon produce 8" x 10" photos, in color and in B/W, of each of the MPC79 die-types. We'll send some copies of these photos to each university, along with info on how to order more copies from the photographer, and how to arrange for individual project photos to be made.

LOOKING AHEAD:

Many of the MPC79 designers are already looking ahead, making plans for iterating their designs, and dreaming up more ambitious design projects. Many other university students will want access to VLSI implementation, so that they too can have the experience of learning to design in a state-of-the-art technology by actually doing it. The demand for such services may build rapidly, once folks know that it is feasible, and can visualize how small is the expenditure of resources per chip-set when compared to the value of the result to the community of designers. Thus, those designers who'd like to iterate their present designs, or take on a larger design, should take heart! There may be several MPC's in 1980! You instructors, coordinators, and designers can help to make sure this happens by letting other folks know what you've done, and how it was done. You can also help us

in this effort by submitting test results and short-form project reports for the MPC79 proceedings.

It is our sincere hope that MPC79 has provided a sufficient demonstration of the feasibility and practicality of remote-entry, fast-turnaround VLSI implementation, that it will lead to the funding and operation of a regular, scheduled VLSI implementation service for university students and researchers. We believe such a service will achieve an enormous return to the country on its investment, by greatly leveraging the human resources to be applied in the exploration of integrated system architecture and design.

ACKNOWLEDGEMENTS:

We wish to express our gratitude to all the folks who pulled together with us to make MPC79 happen, including our friends at Defense ARPA, at Micro Mask, and at Hewlett-Packard/ICPL.

We all owe a great deal to the dedication and efforts of the instructors and lab coordinators in the universities, who, working under great pressure and on a tight schedule, have done such a fantastic job with their design courses and project-labs this fall. We especially want to thank all the student designers for their enthusiastic response to the courses, and for their magnificent efforts and accomplishments on their VLSI system design projects. You have done well!

Organizing and carrying out the implementation of these many imaginative VLSI design projects has been a very exciting and rewarding experience for us here at Xerox PARC/SSL.

The MPC79 Organizers

Lynn Conway, Alan Bell, Martin Newell, Dick Lyon
LSI Systems Area, Xerox PARC/SSL
5 January 1980

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, CA 94304
February 28, 1980

To the MPC79 instructors
and project coordinators:

Dear Friends,

The photomicrographs of the MPC79 chip set have arrived! Enclosed with this shipment are several 8"x10" full-die photographs for you (in color, and in black and white) of each MPC79 die-type that contained projects from your university. Also enclosed are order forms that you and the participants can use to order either full-die photographs, or photographs of individual projects.

I'd appreciate it very much if you would post one set of these photos, and distribute the associated ordering information, so that the MPC79 participants at your university can obtain photos of their projects. Melgar Photographers, the firm that took the photos, specializes in IC photography. Their photographs are of high quality, a wide variety of sizes is available, and they are making the photos available to the MPC79 participants at a very nominal charge.

Also enclosed with this shipment are *Xerox color copies* of the MPC79 die-types containing projects from your university. Enough color copies are enclosed to provide each MPC79 participant from your university with a full set. These color copies don't have the resolution and quality of the original color photos, and certainly don't show as much detail of individual projects as will individual project photos ordered from Melgar. However, I think they will be of interest to the MPC79 participants, and I'd appreciate it if you would distribute them to as many MPC79 participants as possible at your university.

We are also sending (either with, or in parallel with, this shipment) some more unpackaged MPC79 chips for distribution to participants; there are about three chips in the shipment for each project from your school. If mounted in plastic boxes, these unpackaged chips provide a handy way to study the projects with microscopes, and make good souvenirs for the MPC79 participants.

We're working on the various MPC79 documents and reports, and will distribute copies of these to you as soon as they become available.

Sincerely,

Lynn Conway

Lynn Conway