Implementation Documentation for the MPC79 Multi-University Multiproject Chip-Set

A Collection of Information and Instructions conveyed to the Participating Designers, along with their Packaged Chips.

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During the fall of 1979, the LSI Systems Area of Xerox PARC/SSL conducted the demonstration-operation of a prototype system for remote-entry, fast-turnaround implementation of VLSI designs. The user community for this demonstration was composed primarily of EE/CS students taking courses in VLSI system design at many major universities throughout the United States.

A total of 82 VLSI system design projects, created by a total of 124 participating designers, are included in the MPC79 chip-set. Implementation began at the design cutoff-time of 5:00 pm PST, 4 December 1979. Packaged chips, custom wire-bonded for each project, are being distributed to all participants on 2 January 1980. Thus the turnaround time for the MPC79 chip-set was 29 days.

This document provides basic information that the participating designers may use (i) to determine the package-codes for their projects, so as to identify which of the boxed, packaged chips contains their project, (ii) to determine their project pinouts and prepare their chips for testing, (iii) to estimate the maximum clock rates for their projects, (iii) to study the details of the starting frame, and (iv) to learn more about the other participants and the general results of this happening.

Some plans for further documentation and publication concerning MPC79 are also described. Included is a request for short reports (an example short report is appended) from those who'd like to see their projects featured in an upcoming *MPC79 Proceedings*. Many of the projects included in MPC79 have very imaginative, innovative architectures and novel design features. We strongly encourage the designers of such projects to seek publication of their work in the technical journals.

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2. Some Basic Instructions for the Designers
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