2. Some Basic Instructions for the Designers:

This section contains practical information that designers may use (i) to figure out which of the boxed, packaged chips is theirs, (ii) to become aware of cautions to observe when handling their chips, (iii) to determine the pinout of their project, and (iv) to prepare their project for testing.

How to find the packaged chip containing your project

Each MPC79 project has a unique Wafer-type/Die-type/Project-number code, as a function of where that project is physically located on the wafers (for example, Project number 5, on Die-type K, from Wafer-set B, is labelled "BK-5"). Each packaged chip is labelled with the Wafer-type/Die-type/Project-number code of the project within the chip that is bonded to the package leads. The plastic box holding the packaged chip, and the chip package itself are both labelled with this code.

You can find the code for your project in the lists in Section 3 of this document, where these codes are associated with the MPC79 Project IDs (ex: project "BK-5" has the ProjectID "Clark2SU", and belongs to Jim Clark of Stanford University). So, all you have to do to find your packaged chip is look up the code in the lists in Section 3, and then locate the box marked with that code. You should also obtain the custom wire-bonding map marked with your code.

Do be careful when handling the chips

Use caution when handling the boxed chips. Avoid opening and closing the boxes unnecessarily, in order to avoid accumulation of dust and dirt on the chip within. Dust and dirt, although not necessarily damaging to the chips, mars their appearance under microscopes and in photographs. (Note that the chips can be studied under low-power stereo microscopes by looking right through the plastic box cover, with the cover closed). If you open and close the boxes often, even in a dust free environment, an accumulation of tiny white plastic blobs will build-up inside the box and on the chip (these come from the box catch). These won't hurt anything, but they look rather wierd under the microscope. These blobs, and dust particles, can be cleared off the chip's surface (to prepare for photos, etc.) by carefully blowing air over the surface with a plastic squeeze bottle.

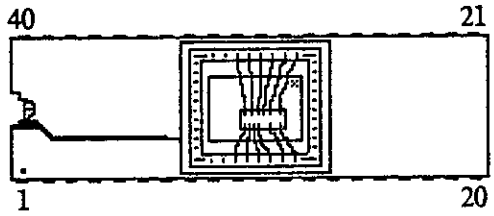
Be *especially* careful when handling your project chip outside of the box, *so as to avoid breaking or shorting the bonding wires.* When you are ready to test your project, and especially if you intend to place it in operational use, you should fashion some sort of removable cover to tape over the package cavity. *However, if you do cover the cavity, be sure not to press down on the bonding wires.* In some cases the bonding wires protrude above the plane of the package surface. Provision of a workable cavity cover will require some ingenuity in such cases.

Until and unless you prepare your project for testing, it is best to keep it in its plastic box. Note that the piece of cardboard wrapped around the package does two things: It provides a tight fit for the package, keeping it from sliding around inside the plastic box, and it also prevents the bonding

wires from being smashed by the box cover. So, install the cardboard wrapper on the package before inserting the package into its plastic box.

Preparing your chip for testing

There are a few simple steps required to prepare your project for testing. First, you will have to figure out your project's package-pinout, in order to know how to interface it to your test equipment. A custom wire-bonding map for each project has been returned with the packaged chips. Find the one with your project code. That map will show how your project has been wire-bonded to the package leads. The map will enable you to deduce the association of project-pads and package pin-numbers. To locate particular package pins, use the following pin locator diagram:



The diagram shows the top view of a ceramic, 40-pin, sidebrazed package having a cavity size of 340 x 340 mils, containing an MPC79-sized project chip (of die-type "X"). One project is bonded-up to the package leads, with wires bonded to leads 9-14, and 27-32. The sketch indicates the positions of the external package pins, with Pin 1 in the lower-left marked by a dot on the package.

The package has some interesting features: Pin 1 is connected to the metal base of the cavity in which the chip is glued (using conductive epoxy). Thus Pin 1 can be used to ground the substrate, or to set it to some particular negative bias. However, it is OK to leave Pin 1 unconnected (if you don't hook-up Pin 1 to some external connection, the substrate will float down to some modest negative voltage during operation of the chip). If it is necessary to use all 40 pins, then the Pin 1 connection to the substrate can be broken by breaking off the "breakaway notch" at the left end of the package. Two of the MPC79 projects use all 40 pins, and require this notch to be broken. One MPC79 project, AF-1, has 48 bonding pads, and will be mounted in a different type of package.

Now, you'll note that each row of package pins are all hooked together by a metal strip. These strips are an artifact of the package manufacturing process. In order to prepare the package for insertion into test fixtures, you'll have to cut these metal strips off the pins. This is easily done using a set of sturdy, sharp scissors, or a pair of sharp metal-nippers. To keep the package from sliding around in its box following removal of these strips, place some plastic foam in the box (and unless a cover has been placed over the package cavity, continue to use the cardboard wrapper).

If you plan to leave your chip installed in test circuitry for any period of time, it's a good idea to tape some sort of cover over the cavity (but be careful not to press down on the bonding wires!). This will protect the chip and the bonding wires. The cover may also be necessary in certain cases to reduce the light reaching the chip during in-circuit operation (see Mead & Conway, p. 134).

The starting frame and electrical test data later in this document will help you estimate the expected maximum clock rate of your project. Your chip is now ready for functional testing!

Selecting chips for further packaging

In addition to the boxed, packaged chips, we've shipped some unpackaged chips to each school. More will be returned in the coming months. Lab coordinators or designers having access to packaging facilites may wish to package some of these chips. To select chips for packaging a particular project, first find some chips of the correct die-type code (the die-type code is indicated by a large letter in the upper-right corner of each chip). Then make an optical inspection under a high-power microscope of the desired project on each of the chips. You may want to make this inspection after the chips are mounted in packages, to detect any damage caused during mounting. If no obvious defects are seen in that project on a chip, then that chip is suitable for the bonding of the project. If there is an obvious defect in that project on a chip, that chip is not discarded but is instead returned to the collection of unpackaged chips (perhaps marked in some way), because other projects on the chip may be OK. The quality of wafer fabrication for MPC79 is excellent, relative to the value of λ, and so this optical inspection may not be necessary for small projects.

When selecting diced chips for further packaging, note whether or not they are overglassed. Chips that are overglassed and have their package-cavities covered are well protected from possible contaminants, and can be placed into long term use. A small fraction of the wafers have been overglassed, so that any projects that function correctly can be placed into such long term use. However, even non-overglassed chips have relatively long-term functional lifetimes (a number of years), if they are kept boxed or covered and kept away from exposure to humid, salty atmospheres. The overglassing of chips sometimes visually obscures the details of the fabricated circuitry. Thus most of the MPC79 wafers will not be overglassed, so that projects can be more clearly studied and photographed through microscopes. In addition, non-overglassed chips can be internally probed if necessary for functional debugging. So, you're probably better off initially with non-overglassed chips. If your project works, you might have some overglassed chips packaged-up later.

Using the microscope to look at and show off your chip

It is always thrilling to take your first look through a microscope at a newly-implemented project that you have designed. It's almost magical to see, printed in fine detail on silicon, the project you spent all those long hours working on. If you want to see all the details of your project and how well the process worked, you will need a high-power microscope. This may help you to uncover various design rule errors, etc., that you hadn't noticed before (note that many chips will work even with slight technical design-rule errors, since the value of λ was conservative). Use unpackaged chips for this purpose, so as not to take a chance of smashing the bonding wires of your packaged chips. We strongly recommend that you also take a look at your chip using relatively low-powered stereo microscopes. Although you can't see fine detail with these, they provide more of an overview of project chips, and are a good way to show them off and explain them to others. You can also use these to confirm that the wire-bonding of your chip was properly done. You can obtain nice interference colors when using stereo microscopes, or even hand magnifiers, by shining light at a moderately low angle across the chip's surface, and rotating the chip very slowly until it is in a position where the colors appear. Under the right conditions, the circuitry will appear to "glow with color" and you will be able to see all the different layers, in different colors!