

# Documentation for Participants in the MPC580 Multiproject Chip-Set

A Collection of Information and Instructions conveyed to the Participating Designers,  
along with their Packaged Chips.

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7 July 1980

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## **A special acknowledgement from Ted Strollo**

MPC580 is a follow on to the very successful MPC79 effort. It would not have been possible without the incredible behind the scenes help from the SSL - LSI people - especially Lynn Conway, Alan Bell, Richard Lyon, and Martin Newell. I also want to extend my thanks to the members of my group (VCI) who helped pull this off - Kevin Gillette, Glenn Krasner, Maureen Stone, and Wayne Wilner. While I signed off on all the formal MPC580 communications, it was this team effort that made MPC580 happen. To every member of this team I extend my personal gratitude and love.

## **Forward**

A total of 171 VLSI system design projects, created by 15 universities/organizations, are included in the MPC580 chip-set. This is an amazing growth from the 82 projects in MPC79, and we expect this appetite for custom VLSI system design projects to continue to grow!

This document provides basic information that the participating project coordinators and designers may use (i) to determine which packaged project belongs to which designer(s), (ii) to determine their project pinouts and prepare their chips for testing, (iii) to estimate the maximum clock rates for their projects, (iii) to study the details of the starting frame, and (iv) to learn more about the projects of the other participants.

## **List of Sections:**

1. Introduction and Overview
2. Some Basic Instructions for the Designers
3. List of Designers and Their Projects
4. Starting Frame Documentation
5. Electrical & Process Measurements
6. Request for Feedback and Further Plans

# 1. Introduction and Overview

This introductory section provides background information about MPC580. Summaries are provided of the participants, of the organizations involved in the implementation effort.

Section 2 contains important basic information that the designers can use to prepare the chips for testing. Section 3 contains a complete list of all projects and designers. Sections 4 and 5 provide information about the starting frame and electrical test results. Finally, Section 6 discusses our plans for packaging and distributing more chips, and for distributing chip photographs.

## The Background and Context of MPC580

Early in 1980, a new group, VCI (VLSI Computer Integration) was formed within the Systems Science Laboratory (SSL) at the Xerox Palo Alto Research Center (PARC). This group has several missions. Two of these are:

- a) To help the external to Xerox community get MPC services for 1980.
- b) To transfer the support of the ARPA sponsored university MPC services to an ARPA contractor - specifically USC-ISI (University of Southern California, Information Sciences Institute).

## The Participants in MPC580

The user community for this multi-project chip set was composed primarily of EE/CS students taking courses in VLSI system design at major universities throughout the United States, along with a number of university faculty and research staff members undertaking major VLSI system designs. In addition, ARPA sponsored a few non-university organizations.

The MPC580 chip set contains a total of 171 VLSI system design projects from a total of 15 participating organizations. Designs were included from BBN (Bolt Beranek and Newman, Inc.), Caltech, CMU, ISI, JPL (Jet Propulsion Laboratory), M.I.T., Stanford University, Univ. of California at Berkeley, UCLA, Univ. of Colorado, Univ. of Illinois, Univ. of Rochester, USC, Washington Univ. at St. Louis, and a few test patterns and "pictures" from Xerox PARC.

## Organizations involved in the implementation effort

Several other organizations collaborated closely with us: Data communications (electronic messages, design file transfers) were supported using the ARPANET for the ARPA supported organizations - the GTE Telenet for the Xerox supported organizations; wafer fabrication was done by Hewlett-Packard's Integrated Circuit Processing Laboratory; ISI helped us substantially with the reading and writing of magnetic tapes and with some of the preparation of this document; maskmaking was done by Micro Mask, Inc., using an electron-beam maskmaking system; and packaging was done by Systems Concepts Inc utilizing equipment at Xerox PARC's Integrated Circuits Lab.

For an overview of the flow of information and artifacts through these various organizations, see the MPC580 Flowchart at the end of this section.

## MPC580 implementation schedule and details

MPC580 had a scheduled project submission cutoff time of 1700 PDT on May 30, 1980. We attempted to run MPC580 as a spooler with new project requests being accepted as early as April 15, 1980 and implement requests being accepted as early as May 1, 1980. What actually happened was an enormous surprise to us. Virtually everyone waited until the last minute. Undoubtedly people were checking designs as carefully as they could before final submission for implementation. The pace on May 29 and 30 was quite frantic for us as we tried to keep up with the requests. Unfortunately, we had some hardware reliability problems with the PARC-MAXC computer which had us off the net for approximately a 9 hour period in the last 24 hours of MPC580. We informally extended the deadline to approximately 2200 on May 30. The valiant efforts of Alan Bell, Kevin Gillette, and Maureen Stone during those final frantic hours were invaluable to the successful completion of MPC580. Ted Strollo finally shut down MPC580 at 2252 PDT on May 30. Each project coordinator was sent a copy of his/her status file.

When we finished, there were 4 projects that were in the open but not ready state. One of these was an initial handshake, a test file transmission not intended to be implemented. The other 3 were projects for which we received new project requests but no further messages. Since none of the project coordinators has told us we missed anything, we are assuming these 3 just didn't get any further into the pipeline than getting an ID assigned.

With MPC580 we experimented with offering designers 2 values of lambda, 2.5 microns and 2.0 microns. Most projects (in fact all those in the first 4 wafer runs) were done at lambda of 2.5 microns. A few projects required the smaller value of lambda of 2.0 microns for either circuit size or speed considerations. These were implemented on the MPC580 5th wafer run.

Micro Mask and Hewlett-Packard gave us astonishingly fast turn around. MPC580 filled up 5 (FIVE) mask sets as compared with 2 (TWO) for MPC79. Micro Mask had early masks for us on 11 June 1980. All of the remaining masks for the first 4 runs were at HP within a week from that date thus HP was able to begin pipelining all 4 wafer runs. HP expects to have the first wafer runs back to us the week of July 7. We plan to ship packaged chips out of PARC the week of July 14. At this writing, we are not finished with all the fab/packaging/shipping cycle (The final set of masks for the fifth run which is lambda of 2 microns was delivered to HP June 30) but we expect it to be completed by approximately the end of July 1980.

### Looking Ahead

The demand for VLSI implementation services will clearly increase. We are pleased to be part of the technology transfer of this service to ISI for the ARPA sponsored sites. There will be another run (tentatively scheduled for cut off January 30, 1981). With this run, the electronic mail and file transfers will be direct to ISI with Xerox assisting in the overall coordination of the effort.

### Acknowledgements

We wish to express our gratitude to everyone who pulled together with us to make MPC580 happen, including Defense ARPA, ISI, Micro Mask, Hewlett-Packard/ICPL, Systems Concepts Inc, and Xerox Corporation for being so supportive of the effort. We all owe a great deal to the dedication and efforts of the instructors and project coordinators in the universities and

participating organizations, who, working under great pressure and on a tight schedule, have done such a fantastic job. We especially want to thank all the designers for their magnificent efforts and accomplishments on their VLSI system design projects. You have done well, and it has been our pleasure to serve you.

#### **A Dedication**

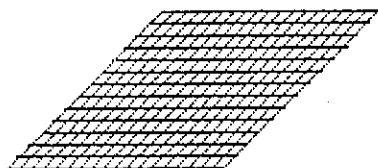
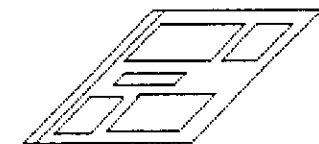
As organizer of MPC580, I, Ted Strollo, am dedicating the MPC580 project to Bill Plummer whose picture actually got imaged in the unusable for circuits area of the metal layer on wafer set D\*. Bill provided the inspiration for a few fun hacks during MPC580, and, were it not for the fun and enjoyment I got out of those hacks, I might never have made it through to the completion of this effort. Many thanks to you Bill, you made it all worth while!

\*A picture of Alan Bell also got similarly imaged on wafer sets A,B, and C

# MPC580 FLOWCHART

(symbol PLACONNECT);  
DS 42 250 10;  
L ND; W 20 35,0 80,0;  
...  
L NM; W 40 35,-75 35,75;  
DF;

TO: MPC580@PARC-MAXC  
FROM: COHEN@USC-ISIB  
SUBJECT: IMPLEMENT MORSEISI



Designers from BBN, U. C. Berkeley, Caltech, CMU, ISI, JPL, MIT, Stanford, UCLA, U of Colorado, U of Illinois, U of Rochester, USC, Washington U St. Louis, Xerox, ...

Project lab coordinators at each school use local electronic mail and file transfer facilities to interact with the designers and used the ARPANET and GTE TELENET to interact with MPC580.

COMMUNICATIONS NETWORKS  
(Mail systems, File transfer systems)

Information Management: Xerox PARC/SSL  
Checking, Planning, Merging of designs into starting frames  
Meeting of Constraints, Coordination, Logistics.

Mask Making: Micro Mask Inc.  
Data format: MEBES; ETEC electron-beam system.

Wafer Fabrication: Hewlett-Packard/ICPL  
NMOS Silicon Gate  
LAMBDA = 2.0 and 2.5 microns

Packaging  
Systems Concepts Inc., using Xerox/ICL equipment

Packaged chips, custom wire bonded per project, along with plots, wire bonding maps, and results of electrical testing, to send back to the designers for functional testing.

## 2. Some Basic Instructions for the Designers:

This section contains practical information that designers may use (i) to figure out which of the boxed, packaged chips is theirs, (ii) to become aware of cautions to observe when handling their chips, (iii) to determine the pinout of their project, and (iv) to prepare their project for testing.

### How to find the packaged chip containing your project

Each packaged MPC580 project has two ways by which you may identify it. Each packaged chip is labelled with the MPC580 system assigned project ID. In the unlikely event that this label comes off, you can read the wafer/die type ID in the upper right of the starting frame with a very low power magnifier. In fact in the right lighting with good eyesight, you can read these with the naked eye. This ID is two letters. The first letter tells you the wafer set where your project was fabbed (A-E, 1-5 respectively). The second letter designates the die type (A-I for wafers A-D; and A-F for wafer E. All wafers had a die type Y which has a couple of special test projects in them). It is not important that you understand the wafer/die type labelling scheme since in most cases the MPC580 assigned project name will be clearly visible on the package. Section 3 has a list of all projects by MPC580 assigned project name and with the wafer/die type ID information. The marked up bonding map delivered with each project further identifies the project within the die type. In addition, we have included, for completeness, the layouts of projects within each die in section 3.

### Do be careful when handling the chips

Use caution when handling the boxed chips. Avoid opening and closing the boxes unnecessarily, in order to avoid accumulation of dust and dirt on the chip within. Dust and dirt, although not necessarily damaging to the chips, mars their appearance under microscopes and in photographs. (Note that the chips can be studied under low-power stereo microscopes by looking right through the plastic box cover, with the cover closed). If you open and close the boxes often, even in a dust free environment, an accumulation of tiny white plastic blobs will build-up inside the box and on the chip (these come from the box catch). These won't hurt anything, but they look unusual under the microscope. These blobs, and dust particles, can be cleared off the chip's surface (to prepare for photos, etc.) by carefully blowing air over the surface with a plastic squeeze bottle.

Be *especially* careful when handling your project chip outside of the box, *so as to avoid breaking or shorting the bonding wires*. When you are ready to test your project, and especially if you intend to place it in operational use, you should fashion some sort of removable cover to tape over the package cavity. *However, if you do cover the cavity, be sure not to press down on the bonding wires*. In some cases the bonding wires protrude above the plane of the package surface. Provision of a workable cavity cover will require some ingenuity in such cases.

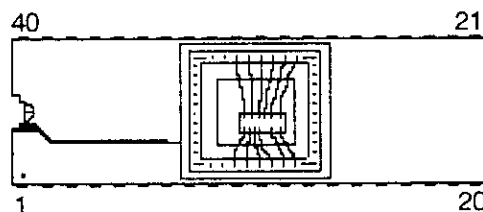
We do have package lids at PARC. These are normally installed in special equipment in a nitrogen gas environment. We do not have this equipment at PARC. It will be unusual for a project to

require this type of lid, but we can provide a limited number of these on request.

Until and unless you prepare your project for testing, it is best to keep it in its plastic box. Note that the piece of cardboard wrapped around the package does two things: It provides a tight fit for the package, keeping it from sliding around inside the plastic box, and it also prevents the bonding wires from being smashed by the box cover. So, install the cardboard wrapper on the package before inserting the package into its plastic box.

#### Preparing your chip for testing

There are a few simple steps required to prepare your project for testing. First, you will have to figure out your project's package-pinout, in order to know how to interface it to your test equipment. A custom wire-bonding map for each project has been returned with the packaged chips. Find the one with your project code. That map will show how your project has been wire-bonded to the package leads. The map will enable you to deduce the association of project-pads and package pin-numbers. To locate particular package pins, use the following pin locator diagram:



The diagram shows the top view of a ceramic, 40-pin, sidebrazed package having a cavity size of 340 x 340 mils, containing an MPC580-sized project chip (wafer A-D sized). One project is bonded-up to the package leads, with wires bonded to leads 9-14, and 27-32. The sketch indicates the positions of the external package pins, with Pin 1 in the lower-left marked by a dot on the package.

The package has some interesting features: Pin 1 is connected to the metal base of the cavity in which the chip is glued (using conductive epoxy). Thus Pin 1 can be used to ground the substrate, or to set it to some particular negative bias. However, it is OK to leave Pin 1 unconnected (if you don't hook-up Pin 1 to some external connection, the substrate will float down to some modest negative voltage during operation of the chip). If it is necessary to use all 40 pins, then the Pin 1 connection to the substrate can be broken by breaking off the "breakaway notch" at the left end of the package. Several MPC580 projects either require more pins or are too large for this particular 3M package. We are using a variety of Kyocera and 3M packages and chip carriers for accomodating these (eq all those projects in the wafer E run - there the chip size is large).

Now, you'll note that each row of package pins are all hooked together by a metal strip. These strips are an artifact of the package manufacturing process. In order to prepare the package for insertion into test fixtures, you'll have to cut these metal strips off the pins. This is easily done using a set of sturdy, sharp scissors, or a pair of sharp metal-nippers. To keep the package from sliding around in its box following removal of these strips, place some plastic foam in the box (and unless a cover has been placed over the package cavity, continue to use the cardboard wrapper).

If you plan to leave your chip installed in test circuitry for any period of time, it's a good idea to tape some sort of cover over the cavity (but be careful not to press down on the bonding wires!). This will protect the chip and the bonding wires. The cover may also be necessary in certain cases to reduce the light reaching the chip during in-circuit operation (see Mead & Conway, p. 134).

The starting frame and electrical test data later in this document will help you estimate the expected maximum clock rate of your project. Your chip is now ready for functional testing!

### **Selecting chips for further packaging**

In addition to the boxed, packaged chips, we've shipped some unpackaged chips to each project coordinator. Lab coordinators or designers having access to packaging facilities may wish to package some of these chips. To select chips for packaging a particular project, first find some chips of the correct wafer and die-type code; then make an optical inspection under a high-power microscope of the desired project on each of the chips. You may want to make this inspection after the chips are mounted in packages, to detect any damage caused during mounting. If no obvious defects are seen in that project on a chip, then that chip is suitable for the bonding of the project. If there is an obvious defect in that project on a chip, that chip is not discarded but is instead returned to the collection of unpackaged chips (perhaps marked in some way), because other projects on the chip may be OK. The quality of wafer fabrication for MPC580 is excellent, relative to the value of  $\lambda$ , and so this optical inspection may not be necessary for small projects.

When selecting diced chips for further packaging, note whether or not they are overglassed. Chips that are overglassed and have their package-cavities covered are well protected from possible contaminants, and can be placed into long term use. A small fraction of the wafers have been overglassed, so that any projects that function correctly can be placed into such long term use. However, even non-overglassed chips have relatively long-term functional lifetimes (a number of years), if they are kept boxed or covered and kept away from exposure to humid, salty atmospheres. The overglassing of chips sometimes visually obscures the details of the fabricated circuitry. Thus most of the MPC580 wafers will not be overglassed, so that projects can be more clearly studied and photographed through microscopes. In addition, non-overglassed chips can be internally probed if necessary for functional debugging. So, you're probably better off initially with non-overglassed chips. If your project works, you might have some overglassed chips packaged-up later.

### **Using the microscope to look at and show off your chip**

It is always thrilling to take your first look through a microscope at a newly-implemented project that you have designed. It's almost magical to see, printed in fine detail on silicon, the project you spent all those long hours working on. If you want to see all the details of your project and how well the process worked, you will need a high-power microscope. This may help you to uncover various design rule errors, etc., that you hadn't noticed before (note that many chips will work even with slight technical design-rule errors, since the value of  $\lambda$  was conservative). Use unpackaged chips for this purpose, so as not to take a chance of smashing the bonding wires of your packaged chips. We strongly recommend that you also take a look at your chip using relatively low-powered stereo microscopes. Although you can't see fine detail with these, they provide more of an overview of project chips, and are a good way to show them off and explain them to others. You can also

use these to confirm that the wire-bonding of your chip was properly done. You can obtain nice interference colors when using stereo microscopes, or even hand magnifiers, by shining light at a moderately low angle across the chip's surface, and rotating the chip very slowly until it is in a position where the colors appear. Under the right conditions, the circuitry will appear to "glow with color" and you will be able to see all the different layers, in different colors!

### 3. List of Designers and Their Projects:

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Summary of designs from BBN, updated 30-May-80 21:36:13

Allocated 41.00 sq-mm

Used 38.68 sq-mm

Remaining 2.32 sq-mm

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ID: CCITBBN [DH] Project Name: CCITT Facsimile Data Compressor

Designer: Julie Sussman

Bounding box = 2886 x 2152 microns, Area = 6.21 sq mm

Description: The chip accepts an input stream of black and white pixels and end-of-line indicators under control of a 4-part bit-at-a-time handshake. It outputs the CCITT encoding of the input stream under control of the same handshake. This prototype handles run-lengths of up to 5 black or 5 white pixels in a row.

ID: CRCBBN [DH] Project Name: CRC-CCITT checksum accumulator

Designer: Norton Greenfeld

Bounding box = 1596 x 1230 microns, Area = 1.96 sq mm

Description: An implementation of the usual multi-section shift register form of the CRC-CCITT polynomial error check circuit. The functionality includes RESET (set all internal bits to 1); INPUT a bit and accumulate checksum; HOLD the current value; READOUT the checksum; and TEST for the magic residual value indicating no errors in the message.

ID: NOISEBBN [DH] Project Name: Noise Generator

Designer: Jack Klovstad, Jerry Wolf

Bounding box = 4586 x 1450 microns, Area = 6.65 sq mm

Description: This pseudo-random noise generator is intended for use in speech synthesis as the source of white noise for unvoiced excitation. The random number generator is described in BSTJ, Nov. 1970, pp. 2303-2310, but we use PLAs instead of the flip-flops and XOR-gates described. The number generated is 11 bits in length, with a period of 33825, but this could be extended easily. The random number is generated in parallel, and there are output pads for each bit to facilitate project testing. In an eventual application, the output would be used by a synthesis filter implemented with bit-serial arithmetic elements, so a parallel-to-serial shift register and serial output are included.

ID: PSWGBBN [DH] Project Name: Programmable Square Wave Generator

Designer: William W. Plummer

Bounding box = 2160 x 1896 microns, Area = 4.10 sq mm

Description: Programmable square-wave generator

ID: STACKBBN [AG] Project Name: Stack Cache

Designer: Harry Forsdick, Rick Schantz

Bounding box = 2758 x 1590 microns, Area = 4.39 sq mm

Description: The purpose of this project is to build a hardware Stack Cache so that references to main memory can be reduced. The operations on the Stack are Reset, Push, Pop and Hold. The Stack accepts one data input value (for Push) and produces three possible data output values: Status (always), Data Out (for Pop) and Data Overflow (for Push).

ID: VLFDBBN [AG] Project Name: Variable Length Field Decoder

Designer: Don Allen, Jerry Burchfiel

Bounding box = 2218 x 2484 microns, Area = 5.51 sq mm

Description: This circuit permits the rapid decoding of extremely bit-efficient representations of computer programs and data.

ID: WOODSBBN [DH] Project Name: Contention Gate

Designer: Bill Woods

Bounding box = 4640 x 2126 microns, Area = 9.86 sq mm

Description: This chip permits a number of processors to compete for the attention of a serving processor over a single communication channel. It handles different requests on a priority basis, with the highest priority message from any source always getting through. The gate takes a 16 bit message and transmits it serially onto the communication line. Each communicating process which is contending for the server would require one such chip. The circuit has the virtue that the highest priority message always gets through -- no channel capacity is lost due to clashes of competitors trying to send at the same time.

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Summary of designs from CALTECH, updated 30-May-80 21:36:13

Allocated 387.00 sq-mm

Used 208.80 sq-mm

Remaining 178.20 sq-mm

ID: AMCALTECH [AC] Project Name: Associative Memory

Designer: Howard Derby

Bounding box = 3306 x 2328 microns, Area = 7.70 sq mm

Description: A memory which allows various operations on its contents.

ID: BYRKETCALTECH [AC] Project Name: Byrket

Designer: University of Washington. Bruce Byrket

Bounding box = 2500 x 1860 microns, Area = 4.65 sq mm

Description: This circuit is designed to interface with inertial sensors. It produces a signal to drive the primary of a microsyn on a gyro or accelerometer and demodulates the output of the secondary of the microsyn and demodulates the output of the secondary of the microsyn. An A/D converter could be included on the chip to make a complete interface between an inertial sensor and the navigation system.

ID: CCRTCCALTECH [CB] Project Name: Chinese CRT Controller

Designer: Kuo Ting Ho

Bounding box = 2664 x 1252 microns, Area = 3.34 sq mm

Description: A CRT controller for the Chinese character set.

ID: CORBINCALTECH [AC] Project Name: Corbin

Designer: University of Washington. Vince Corbin

Bounding box = 2226 x 2004 microns, Area = 4.46 sq mm

Description: This is a partial Ethernet receiver chip that is also designed for testability. It includes the data paths for serial-to-parallel conversion and address recognition, including recognizing the broadcast address. The PLA is a finite-state-machine that controls the decoding and message reception processes. The CRC checker and manchester decoder have yet to be added. The purpose of this chip is to experiment with hardware techniques for improving testability.

ID: DACHIPCALTECH [BG] Project Name: Dachip

Designer: University of Washington. J. Cole

Bounding box = 938 x 938 microns, Area = 0.88 sq mm

Description: This chip is a digital to analog converter after a circuit design suggested by Carver Mead.

ID: DANIELCALTECH [DA] Project Name: Daniel

Designer: University of Washington.

Bounding box = 3336 x 4058 microns, Area = 13.54 sq mm

Description: This circuit is a parallel multiplier. It multiplies two 8-bit positive integers to form a 16-bit product. The chip could easily be extended to perform signed magnitude or 2's complement multiplication with a small amount of internal or external circuitry.

ID: DIFET1CALTECH [AC] Project Name: Difet1  
Designer: University of Washington. John Cole  
Bounding box = 1414 x 1010 microns, Area = 1.43 sq mm  
Description: single transistors comprised of a large number of minimum sized source and drain diffusion areas separated by a single lattice-work gate.

ID: DIFET2CALTECH [BG] Project Name: Difet2  
Designer: University of Washington. John Cole  
Bounding box = 934 x 1010 microns, Area = 0.94 sq mm  
Description: single transistors comprised of a large number of minimum sized source and drain diffusion areas separated by a single lattice-work gate.

ID: DIFETCALTECH [CG] Project Name: Difet  
Designer: University of Washington. John Cole  
Bounding box = 1414 x 1010 microns, Area = 1.43 sq mm  
Description: single transistors comprised of a large number of minimum sized source and drain diffusion areas separated by a single lattice-work gate.

ID: FOOBARCALTECH [DA] Project Name: Self Timed Paging Control  
Designer: Richard Segal  
Bounding box = 1626 x 2126 microns, Area = 3.46 sq mm  
Description: A self timed paged memory control element.

ID: GR2CALTECH [DC] Project Name: GR2  
Designer: Ricky Mosteller  
Bounding box = 3592 x 3334 microns, Area = 11.98 sq mm  
Description: Second version of the powerfull GR stack machine.

ID: HLDCCALTECH [CG] Project Name: High Low Digital Converter  
Designer: Elliot Pines  
Bounding box = 1868 x 1200 microns, Area = 2.24 sq mm  
Description: ECPG - Counterpart.

ID: HLECALTECH [CG] Project Name: Hidden Line Eliminator  
Designer: Terry Ligocki  
Bounding box = 2442 x 1142 microns, Area = 2.79 sq mm  
Description: A counter with tree structured carry chain

ID: HOORNSCALTECH [AC] Project Name: Hoorns  
Designer: University of Washington. F. B. Hoornstra  
Bounding box = 3636 x 916 microns, Area = 3.33 sq mm  
Description: The "Hoornstra" 16-bit NMOS digital correlator is functionally patterned after the TRW TDC1004J 64-bit bipolar digital correlator. Both devices consist of strings of three independently clocked digital shift registers capable of parallel correlations, while both devices output current-sourced analog correlations. However, the TRW device employs TTL static latches for shift registers, whereas the NMOS device is designed with dynamic storage cells.

ID: JCOLECALTECH [DC] Project Name: Jcole  
Designer: University of Washington. John C. Cole  
Bounding box = 2694 x 2178 microns, Area = 5.87 sq mm  
Description: This chip implements a simple algorithm for a constant false alarm rate (CFAR) threshold detector for a radar. A CFAR estimates the standard deviation of the received noise and establishes a threshold proportional to this estimated value. The received signal is compared with this threshold for a target/no target decision.

ID: JEXCALTECH [CB] Project Name: Jex

Designer: University of Washington.

Bounding box = 5452 x 2716 microns, Area = 14.81 sq mm

Description: The VLSI F/D chip contains six asynchronous up count registers, 16 bits wide. - one for each sensor. They are fed parallel into a 16 bit static buffer connected to a parallel out 16 bit tri state output for the data bus. All control is implemented with an on-chip PLA.

ID: KAMCHIPCALTECH [DC] Project Name: KamChip

Designer: Kreg Martin

Bounding box = 3456 x 2196 microns, Area = 7.59 sq mm

Description: NMOS chip design.

ID: KOETHECALTECH [BF] Project Name: Koethe

Designer: University of Washington. Koether

Bounding box = 4550 x 1204 microns, Area = 5.48 sq mm

Description: A dual six bit register chip with bussed tristate outputs for use in an underwater autopilot system.

ID: LARSENALTECH [CG] Project Name: Larsen

Designer: University of Washington. Donn Larsen

Bounding box = 2524 x 2030 microns, Area = 5.12 sq mm

Description: This is a storage array consisting of a "m" words by "n" bit serial/parallel input, serial/parallel output shifting array. The array uses dynamic refresh, serial/parallel input and output select wires a two phase clock and I/O pads. This array is 16 words by 8 bits but could have been any size with a change of two constants in the program. Such a storage array is required for each of the separate sections of the VLSI autopilot to optimize message traffic on a cyclical basis for multiparameter arithmetic, filtering, etc.

ID: LRUCAMCALTECH [CG] Project Name: LRU-CAM

Designer: Telle Whitney

Bounding box = 2420 x 2386 microns, Area = 5.77 sq mm

Description: A translation buffer for virtual memories.

ID: MESSMECALTECH [BF] Project Name: Messme

Designer: University of Washington. Messmer

Bounding box = 2300 x 2772 microns, Area = 6.38 sq mm

Description: 10 4-bit counters with special count control used in an underwater autopilot system.

ID: MOERDYCALTECH [CG] Project Name: Moerdy

Designer: University of Washington.

Bounding box = 4664 x 2888 microns, Area = 13.47 sq mm

Description: This chip multiplies two sixteen bit numbers together. The two numbers are entered 8 bits at a time with the lower bit entered first. Four entry cycles complete the loading of the chip. At this point one of the numbers is stored in register associated with the serial adder cells of the multiplier and the other is stored in shift register. After entering the two numbers the chip automatically starts the multiplication. When the multiplication is complete, the chip issues a signal and the result can be read 8 bits at a time.

ID: MULTIPLIERCALTECH [DA] Project Name: Multiplier

Designer: Bruce Pederson

Bounding box = 5986 x 474 microns, Area = 2.84 sq mm

Description: A digital serial multiplier.

ID: OINC2CALTECH [BG] Project Name: OINC2 Processor

Designer: Dave Johannson

Bounding box = 3168 x 3866 microns, Area = 12.25 sq mm

Description: A second version of the OINC processor.

ID: PERCIFCALTECH [BG] Project Name: Percif

Designer: Jeff Sondeen

Bounding box = 3126 x 2834 microns, Area = 8.86 sq mm

Description: A PERCIF chip.

ID: PWMDICALTECH [CB] Project Name: PWM Digital Interface

Designer: Rick Bozzuto

Bounding box = 2420 x 1666 microns, Area = 4.03 sq mm

Description: A pulse width modulation interface circuit.

ID: RDGCALTECH [BF] Project Name: Rotating Display Generator

Designer: Steven Eaton

Bounding box = 2248 x 1426 microns, Area = 3.21 sq mm

Description: Manipulates data for a digital display.

ID: RUMPHCALTECH [DA] Project Name: FIFORumph

Designer: Dave Rumph

Bounding box = 1544 x 1714 microns, Area = 2.65 sq mm

Description: A FIFO

ID: SAMPLECALTECH [DC] Project Name: Sample

Designer: Dave Johannson

Bounding box = 2136 x 3196 microns, Area = 6.83 sq mm

Description: A test of the Bristle Blocks compiler.

ID: STACALTECH [BF] Project Name: Self Timed Adder

Designer: Martine Savalle, Thierry Watteyne

Bounding box = 1404 x 1060 microns, Area = 1.49 sq mm

Description: A self timed adder.

ID: STDPCALTECH [AC] Project Name: Self Timed Data Path

Designer: Eric Barton

Bounding box = 2854 x 3194 microns, Area = 9.12 sq mm

Description: A self-timed PDP-8 data path section.

ID: STFIFOCALTECH [BF] Project Name: Self Timed FIFO

Designer: Kreg Martin

Bounding box = 2376 x 2126 microns, Area = 5.05 sq mm

Description: A queue to buffer DMA data for a digital display.

ID: STPCALTECH [BG] Project Name: Self Timed Parts

Designer: Chris Lutz

Bounding box = 2720 x 1424 microns, Area = 3.87 sq mm

Description: A collection of self-timed elements for experimentation.

ID: SWICALTECH [BF] Project Name: Single Wire Interface

Designer: John Tanner

Bounding box = 1974 x 2500 microns, Area = 4.94 sq mm

Description: Interface for manipulator sensors.

ID: TOUCHSENSCALTECH [CB] Project Name: Touch Sensor

Designer: John Tanner

Bounding box = 3096 x 2628 microns, Area = 8.14 sq mm

Description: An array processor for processing tactile information. A voltage comparator is included in each cell for pressure transduction.

ID: WELLINCALTECH [DA] Project Name: Wellin

Designer: University of Washington. Welling

Bounding box = 4576 x 1946 microns, Area = 8.90 sq mm

Description: This VLSI circuit is an eight bit serial multiplier featuring built in testability. The hardware is divided into eight identical stages with each stage containing a full adder and a set of shift registers. Timing is synchronized by a set of shift registers between stages. Two sets of testability shift registers and control lines allow data to be input and sampled from each stage independently or from all stages simultaneously. A variable sized multiplicand is multiplied by an eight bit multiplier. The multiplier and multiplicand are input simultaneously with the first output bit occurring after eight bits are shifted in. Thereafter each clock cycle shifts out another output bit until all bits are shifted out. Output will continue as long as data is fed in.

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Summary of designs from CMU, updated 30-May-80 21:36:13

Allocated 113.00 sq-mm

Used 74.24 sq-mm

Remaining 38.76 sq-mm

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ID: BARSHIFTCMU [AE] Project Name: 16-Bit Barrel Shifter

Designer: Mark Stehlik

Bounding box = 3438 x 3428 microns, Area = 11.79 sq mm

Description: This is an implementation of a 16-bit barrel shifter. It uses a 4-bit decoder to determine the shift function (and so requires 40 pads). The design is based on the shifter used in the OM2 Data Path Chip.

ID: BITARRPROCMMU [CH] Project Name: Bit Array Processor

Designer: Ed Frank & Carl Ebeling

Bounding box = 2370 x 2350 microns, Area = 5.57 sq mm

Description: This project is a 3x3 BAP. each cell has one bit of static storage, and can compute its next state as a function of its current state and its eight nearest neighbors. In this design each cell has two functions: 1) tally and 2) shift. The shift function allows us to get data in and out of all cells (slowly). The tally function computes the next state based on the number of neighbors which are on. all cells work in parallel. The BAP can be expanded by interconnecting BAP chips.

ID: BS16BCMU [CH] Project Name: 16-Bit Barrel Shift And Mask

Designer: Jim Gasbarro

Bounding box = 3278 x 2958 microns, Area = 9.70 sq mm

Description: This shifter is capable of doing end around shifts as well as zero fill from both the left and right. This feature enables several of the chips to be cascaded to form larger shifters.

ID: CETTCMU [CH] Project Name: C-Element Timing Tester

Designer: Bob Sproull & Ed Frank

Bounding box = 1928 x 386 microns, Area = 0.74 sq mm

Description: This project uses a C element as a way of measuring some of the performance characteristics of nmos.

ID: DCHIPCMU [DE] Project Name: DataChip

Designer: Satish Gupta

Bounding box = 3630 x 2596 microns, Area = 9.42 sq mm

Description: This chip manipulates the data for each of the memory chips in the 8x8 display. It is a 4-bit bit-slice and many of these can be stacked for displays with more than 4-bits per pixel.

ID: ICSCMU [DE] Project Name: Iterative Cell Switch

Designer: Jin H. Kim & J. Carlos Dangelo

Bounding box = 1510 x 1630 microns, Area = 2.46 sq mm

Description: MANUAL LAYOUT OF HYBRID REDUNDANCY UNIT

ID: PLACMU [DE] Project Name: Control Pla

Designer: Diane Detig

Bounding box = 2052 x 4074 microns, Area = 8.36 sq mm

Description: The pla to control my asynchronous deque. There are 21 output signals generated by the pla. There are 11 control signals for my deque cell, 3 signals for communication to other cells, 4 signals store the internal state, and 3 signals control the temporary state of a cell. There are 14 input signals to the pla. There are 4 internal state, 3 temporary state, 3 communication from other cells, and 4 commands from other states.

ID: POLTEXTCMU [AE] Project Name: Poltext

Designer: M. Ciesielski, W. Maly, & A. Strojwas

Bounding box = 2380 x 2400 microns, Area = 5.71 sq mm

Description: Chip displays text stored in ROM on the 8 character alphanumeric display

ID: SERIALMULTCMU [AE] Project Name: Serial Multiplier

Designer: Alexander Waibel

Bounding box = 1670 x 1034 microns, Area = 1.73 sq mm

Description: 3-bit serial multiplier

ID: TCHIPCMU [DE] Project Name: NETLTestChip

Designer: Hank Walker

Bounding box = 3180 x 3180 microns, Area = 10.11 sq mm

Description: 15 x 15 crossbar for NETL system

ID: UDCOUNTERCMU [CH] Project Name: Up Down Counter

Designer: Dave Touretzky

Bounding box = 2920 x 1006 microns, Area = 2.94 sq mm

Description: up/down counter with ripple carry

ID: VIDBUFCMU [BA] Project Name: Video Buffer

Designer: Satish Gupta

Bounding box = 1006 x 5668 microns, Area = 5.70 sq mm

Description: Video buffer for the 8x8 display.

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Summary of designs from ISI, updated 30-May-80 21:36:13

Allocated 24.00 sq-mm

Used 19.89 sq-mm

Remaining 4.11 sq-mm

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ID: ASTISI [AD] Project Name: Automatic Star Tracker

Designer: Vance Tyree

Bounding box = 1150 x 1480 microns, Area = 1.70 sq mm

Description: This project uses the limited analog capability of the NMOS digital technology to implement an optical sensor that will sense the position of a stellar image and indicate the magnitude of its displacement from a telescope optical axis.

ID: COMBLOCKUSC [AF] Project Name: Combination Lock

Designer: William T. Overman

Bounding box = 1590 x 1620 microns, Area = 2.58 sq mm

Description: A five input, one output finite state machine which implements a combination lock with a fixed combination. The output goes high when the proper sequence of inputs is entered. The implementation consists of a single PLA with key debounce and a clear command included in the PLA programming. The feedback variables have been brought out to output pins for testing. A completely separate circuit generates a two phase non-overlapping clock. The outputs from this circuit can be externally wired to the clock inputs for the finite state machine to make the chip completely self-contained.

ID: DPOMASIB [AD] Project Name: Dual Port Memory Arbitrator

Designer: Richard R. Shiffman

Bounding box = 1366 x 958 microns, Area = 1.31 sq mm

Description: This is a state machine designed to solve the problem of conflicts for memory in a dual port memory system.

ID: MFLUNDH [BB] Project Name: Matched Filter

Designer: Yngvar Lundh

Bounding box = 2074 x 1892 microns, Area = 3.92 sq mm

Description: The matched filter will continuously compare an incoming serial data stream with a key loaded ahead. The key will probably be 8 (or perhaps 16) bits. After a delay of 4 clock cycles a 4-bit (or 5-bit) binary output will supply the number of matched bits.

ID: MORSEISI [AD] Project Name: a morse code keyer

Designer: Danny Cohen

Bounding box = 1906 x 1832 microns, Area = 3.49 sq mm

Description: This device accepts morse keying in terms of Dot and Dash signals and converts them into xmt signals with the proper spacing, and with dash/dot ratio of 3. This device allows some keying-ahead.

ID: PADTESTISI [AD] Project Name: Pad-Test

Designer: Danny Cohen

Bounding box = 1108 x 1080 microns, Area = 1.20 sq mm

Description: This is a test of a clock-pad to produce PHI and PHI-BAR which are guaranteed not to be both HIGH.

ID: SERIALMULTISI [AD] Project Name: SerialMultiply

Designer: George Lewicki

Bounding box = 2422 x 1066 microns, Area = 2.58 sq mm

Description: A serial multiplier for use in a two-dimensional filter or interactive image processing.

ID: STGENISI [AD] Project Name: STGEN

Designer: W. Chiu, G. Finn, J. Lacoss, D. Taylor

Bounding box = 2456 x 1266 microns, Area = 3.11 sq mm

Description: HP DMA State Generator Logic

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Summary of designs from JPL, updated 30-May-80 21:36:13

Allocated 50.00 sq-mm  
Used 48.55 sq-mm  
Remaining 1.45 sq-mm

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ID: MEMINTERJPL [BB] Project Name: Memory Interface

Designer: J. Wawrzynek

Bounding box = 3508 x 3000 microns, Area = 10.52 sq mm

Description: A HAMMING CODED MEMORY INTERFACE BUILDING BLOCK FOR USE IN A FAULT TOLERANT COMPUTER.

ID: SYNGENISI [BC] Project Name: Syndrome Generator

Designer: J. Wawrzynek

Bounding box = 1916 x 1816 microns, Area = 3.48 sq mm

Description: A SUBSECTION OF A HAMMING CODED MEMORY INTERFACE FOR USE IN A FAULT TOLERANT COMPUTER.

ID: TESTCHIPJPL [EE] Project Name: Test Chip

Designer: G. Bates, B. Hubbard, B. Blaes, & T. Griswold

Bounding box = 4678 x 7384 microns, Area = 34.54 sq mm

Description: THIS CIRCUIT CONTAINS EXPERIMENTAL TEST STRUCTURES FOR WAFER ACCEPTANCE TESTING AND YIELD/RELIABILITY ESTIMATION.

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Summary of designs from MIT, updated 30-May-80 21:36:13

Allocated 150.00 sq-mm  
Used 133.94 sq-mm  
Remaining 16.06 sq-mm

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ID: BATALIMIT [BA] Project Name: Zero-Crossing

Designer: John Batali

Bounding box = 5086 x 3876 microns, Area = 19.71 sq mm

Description: Zero crossing detector for image processing

ID: CGMIT [BA] Project Name: Clock Generator

Designer: M. Abbas

Bounding box = 1460 x 1358 microns, Area = 1.98 sq mm

Description: Programmable generator of two-phase clocks.

ID: EBEAM2MIT [BA] Project Name: EBeamTestStructure2

Designer: Dave Shaver

Bounding box = 252 x 916 microns, Area = 0.23 sq mm

Description: None

ID: EBEAMMIT [EB] Project Name: EBeamTestStructure1

Designer: Dave Shaver

Bounding box = 200 x 976 microns, Area = 0.20 sq mm

Description: None

ID: FANCIRCMIT [AE] Project Name: Fancy Circuits

Designer: Mark Johnson

Bounding box = 2044 x 3058 microns, Area = 6.25 sq mm

Description: High speed, low power circuits for output pad, clock driver, substrate bias, and parametric measurements

ID: GLASSERMIT [BA] Project Name: PLA City  
Designer: Lance Glasser  
Bounding box = 2536 x 1360 microns, Area = 3.45 sq mm  
Description: Various PLA's to try out their speed

ID: MAYLEMIT [AE] Project Name: Crossbar  
Designer: Neil Mayle  
Bounding box = 2250 x 2126 microns, Area = 4.78 sq mm  
Description: Crossbar for AI constraint networks

ID: PORTALMIT [CD] Project Name: Portal Chip  
Designer: Phyllis Koton, Carl Hewitt  
Bounding box = 3740 x 5780 microns, Area = 21.62 sq mm  
Description: Packet Interface between processors in a multiple processor system

ID: RIESMIT [CD] Project Name: Fifo  
Designer: Paul Ries  
Bounding box = 1964 x 1918 microns, Area = 3.77 sq mm  
Description: Dual Rail FIFO Buffer

ID: RIVESTMIT [EC] Project Name: Encryption Chip  
Designer: Ron Rivest, Adi Shamir, Len Adleman  
Bounding box = 5732 x 8084 microns, Area = 46.34 sq mm  
Description: RSA Encryption Chip

ID: SECMIT [ED] Project Name: Small Encryption Chip  
Designer: R. Rivest, A. Shamir, L. Adleman  
Bounding box = 3872 x 6614 microns, Area = 25.61 sq mm  
Description: RSA Encryption Chip

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Summary of designs from STANFORD, updated 30-May-80 21:36:13

Allocated	195.00 sq-mm
Used	187.36 sq-mm
Remaining	7.64 sq-mm

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ID: AESTANFORD [CE] Project Name: Adaptive Equalizer  
Designer: Jonathan Green, Robert Jaffee  
Bounding box = 4744 x 2658 microns, Area = 12.61 sq mm  
Description: a 32-tap, 12-bit filter with weights changed adaptively based on an error input using the Widrow-Hoff algorithm

ID: ALU8BSTANFORD [AB] Project Name: 8-Bit ALU  
Designer: Bayegan/Hagiwara  
Bounding box = 1856 x 2026 microns, Area = 3.76 sq mm  
Description: an 8-bit ALU with 2 input sets and 16 operations

ID: ALUTESTSTANFORD [CF] Project Name: AluTest  
Designer: Wayne Wolf  
Bounding box = 2196 x 3146 microns, Area = 6.91 sq mm  
Description: A test of the bit slice ALU.

ID: ASYNFIFOSTANFORD [DD] Project Name: Asynchronous FIFO

Designer: Fenwick, Jahn, Wantzelius

Bounding box = 4310 x 1350 microns, Area = 5.82 sq mm

Description: The project consists of a 4-phase clock generator/clock selector circuit controlling an asynchronous 4-bit by 16-word FIFO. A 1-bit adder circuit is also included.

ID: AWGSTANFORD [DB] Project Name: AudioWaveformGenerator

Designer: Won Kim, John Schur

Bounding box = 3058 x 3878 microns, Area = 11.86 sq mm

Description: This project samples data points in an external RAM at a requested frequency, using a 24 bit frequency specification and interpolating the 12 bit data points to output to a D/A converter.

ID: BLACKJACKSTANFORD [DB] Project Name: Blackjack

Designer: Lori Craven, Don Paulus

Bounding box = 2650 x 2620 microns, Area = 6.94 sq mm

Description: Input = dealer's up card value, player's card values

Output = total of player's cards and hit or done or fold indication

ID: CCTSTANFORD [CE] Project Name: Counter Cell Tester

Designer: J. L. Redford

Bounding box = 1894 x 900 microns, Area = 1.70 sq mm

Description: a test of two counter cells before inclusion in a library

ID: CFIRFSSTANFORD [AB] Project Name: Cascadable FIR Filter Stage

Designer: Rex Heller, Rick Ottolini

Bounding box = 4828 x 1110 microns, Area = 5.36 sq mm

Description: This project is a convolver for on-site data reduction during collection of geophysical field data.

ID: CORSICASTANFORD [DB] Project Name: Corsica

Designer: Newman, Perry

Bounding box = 2536 x 1848 microns, Area = 4.69 sq mm

Description: this project uses the cordic algorithm to compute the sine and cosine of serial input data

ID: DCLOCKSTANFORD [BE] Project Name: Digital Clock

Designer: K. Doganis

Bounding box = 4126 x 1700 microns, Area = 7.01 sq mm

Description: Digital clock using 11 PLA's in series, and a 3-7 decoder drives the MUX.

ID: DRAMCSTANFORD [CF] Project Name: Dynamic RAM Controller

Designer: Marc R. Hannah

Bounding box = 2036 x 1964 microns, Area = 4.00 sq mm

Description: Test of a subsystem to be used in a graphics processor.

ID: DTUSTANFORD [CF] Project Name: Digital Timer Unit

Designer: k. wagner, c. caulfield

Bounding box = 2988 x 2254 microns, Area = 6.73 sq mm

Description: digital timer with stop/start reset that counts up to 100 minutes - unit to be used as a 'split' timer

ID: EDCSTANFORD [DD] Project Name: ERROR DETECTION & CORRECTION CIRCUITRY FOR RAM

Designer: S. Z. Hassan, A. Mahmood, K. A. Kamal

Bounding box = 1990 x 1454 microns, Area = 2.89 sq mm

Description: The project is concerned with the detection and correction of random errors in RAMs.

ID: FREDSTANFORD [BE] Project Name: Fred  
Designer: Borriello, Gaetano, and French, Paul  
Bounding box = 1746 x 4896 microns, Area = 8.55 sq mm  
Description: Graphics Memory - Stores coordinates of rectangles on a screen (4 types of shading) and supplies the boolean value of a pixel when supplied with the screen coordinates.

ID: IIRDFSTANFORD [DB] Project Name: 2nd Order IIR Digital Filter  
Designer: Amnon Aliphas, Frank Soong  
Bounding box = 3000 x 2650 microns, Area = 7.95 sq mm  
Description: A ROM table lookup multiplication is used in this IIR filter implementation. Input data samples and output samples involved in the computation of the recursive filter equation:  
$$y(n) = a_0x(n) + a_1x(n-1) + a_2x(n-2) - b_1y(n-1) - b_2y(n-2)$$
  
will be stored in dynamic registers.

ID: M6800STANFORD [CE] Project Name: Motorola M6800 Co-Processor  
Designer: Alain Guyot, Neville Harris  
Bounding box = 2586 x 1652 microns, Area = 4.27 sq mm  
Description: None

ID: MULTTESTSTANFORD [DD] Project Name: Multiplier Test  
Designer: Lyle Smith  
Bounding box = 2948 x 2320 microns, Area = 6.84 sq mm  
Description: Test of Lyon's multiplier and a serial adder

ID: MULTSTANFORD [CE] Project Name: Multiplier  
Designer: M. Ferrazano, S. Midkiff  
Bounding box = 2228 x 1520 microns, Area = 3.39 sq mm  
Description: A 4x4 to 8 Booth's Algorithm Multiplier

ID: MYCHIPSTANFORD [BE] Project Name: MYChip  
Designer: Lena Yesil, Steve Morley  
Bounding box = 2404 x 2446 microns, Area = 5.88 sq mm  
Description: Two's complement multiplier using Booth's algorithm

ID: NEURONSTANFORD [CE] Project Name: Neuron  
Designer: Wayne Wolf  
Bounding box = 1764 x 2516 microns, Area = 4.44 sq mm  
Description: A pair of neuron emulators.

ID: NUKESTANFORD [CF] Project Name: Library test chip  
Designer: John Newkirk  
Bounding box = 3756 x 1434 microns, Area = 5.39 sq mm  
Description: This chip is a test of up/down counter, comparator, dual-port register, and geometric-distribution random-number generator cells contributed by Hahn et al.

ID: PFMSTANFORD [DD] Project Name: Programmable Frequency Multiplier  
Designer: David Beal, James Ferenc  
Bounding box = 1590 x 1326 microns, Area = 2.11 sq mm  
Description: This project is a programmable  $2^{**n}$  frequency multiplier. The input consists of a square wave of frequency  $f$ . The output is then a 50% duty cycle square wave of frequency  $(2^{**n})f$ . The value  $n$  is a two bit number specified by the user.

ID: PGSTANFORD [AB] Project Name: Pattern Generator  
Designer: Kenneth Ng Yu, Tahn-Joo Tan  
Bounding box = 2500 x 2566 microns, Area = 6.42 sq mm  
Description: None

ID: PHASEDECSTANFORD [EB] Project Name: Phase Decoder

Designer: Forrest Baskett

Bounding box = 1792 x 2176 microns, Area = 3.90 sq mm

Description: a phase decoder for implementing Ethernet, hopefully functional at speed this time

ID: PICSTANFORD [AB] Project Name: Programmable Interface Controller

Designer: Ang/Yuen

Bounding box = 2030 x 2406 microns, Area = 4.88 sq mm

Description: This project is a programmable interface controller that sits on a microprocessor bus.

ID: PMULTSTANFORD [AB] Project Name: Parallel Multiplier

Designer: Levis, Tinker

Bounding box = 2476 x 1910 microns, Area = 4.73 sq mm

Description: Pipelined parallel multiplier/adder. Computes  $R = AB + C$  where A is a 4 bit 2's complement fraction, and R, B, and C are 8 bit 2's complement integers. The low order product terms are truncated.

ID: POTATOSTANFORD [DD] Project Name: Potato Chip

Designer: Hunt, Lozano, Hahn

Bounding box = 4500 x 3250 microns, Area = 14.63 sq mm

Description: P-CSMA/CD network interface.

ID: PSDSTANFORD [BE] Project Name: Programmable Sequence Detector (PSD)

Designer: D. Thompson, P. Decher

Bounding box = 1840 x 1344 microns, Area = 2.47 sq mm

Description: This chip is a programmable digital comparator that can monitor either a parallel or a serial data line.

ID: RANDOMSTANFORD [AB] Project Name: Random chip

Designer: K. Karplus, A. Strong

Bounding box = 1810 x 1416 microns, Area = 2.56 sq mm

Description: A feedback shift register random number generator, has extra "decay bit" with programmable probability of being hi [A functional subunit of the guitar chip.]

ID: SDRTSTANFORD [BE] Project Name: Serial data receiver and transmitter

Designer: Roy Matsuyama, Mark Phillips

Bounding box = 2376 x 2626 microns, Area = 6.24 sq mm

Description: we are designing a four bit serial data receiver and transmitter which operate independently of each other.

ID: SMSTANFORD [CE] Project Name: Switch Matrix

Designer: Saied Bozorgui-Nesbat, Steve Butner

Bounding box = 1766 x 2390 microns, Area = 4.22 sq mm

Description: 4 X 4 switching matrix --- any input line (or its complement) may be ORed-in to any output line. Any output line may be complemented. Uses include programmable NOR gates, programmable PLA (requires 2 units), point-to-point switching, or programmable FSMs (requires 2 units).

ID: TICTACSTANFORD [CF] Project Name: TicTac

Designer: Aviles, Woodson

Bounding box = 3588 x 2288 microns, Area = 8.21 sq mm

Description: this is a tic-tac-toe player

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Summary of designs from SPECIAL, updated 30-May-80 21:36:13

Allocated 212.00 sq-mm  
Used 98.99 sq-mm  
Remaining 113.01 sq-mm

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ID: ALANSPECIAL [AI], [BI], [CI] Project Name: Alan Picture  
Designer: Strollo  
Estimated Bounding box = 5750 x 5750 microns, Area = 33.06 sq mm  
Description: Picture of Alan Bell which appeared in Lambda. DO NOT ROTATE.

ID: BILLSPECIAL [DI] Project Name: Bill Picture  
Designer: Strollo  
Estimated Bounding box = 5750 x 5750 microns, Area = 33.06 sq mm  
Description: Picture of Bill Plummer and Ann Tomlinson. DO NOT ROTATE.

ID: HPTESTSPECIAL [AY], [BY], [CY], [DY], [EY] Project Name: HPTest  
Designer: Wilner  
Bounding box = 4000 x 3000 microns, Area = 12.00 sq mm  
Description: These are the twelve test patterns designed by Xerox to be compatible with an HP test system. They need only appear once on each die.

ID: MultSpec [CC] Project Name: Mult580  
Designer: Lyon  
Bounding box = 5954 x 2556 microns, Area = 15.22 sq mm  
Description: Pair of 16-bit mults w/ extras. Do not rotate if possible.

ID: TALLYSPECIAL [DG] Project Name: Tally580  
Designer: H. Landman  
Bounding box = 1554 x 1490 microns, Area = 2.32 sq mm  
Description: A tally circuit a la Mead & Conway. The one I did for the 8/79 internal MPC was found not to work even though everyone (including Dick Lyon & Alan Bell) who looked at it believed it to be correct. This one will try to find out why.

ID: TP580SPECIAL [AY], [BY], [CY], [DY], [EY] Project Name: TP580  
Designer: Landman  
Bounding box = 1000 x 570 microns, Area = 0.57 sq mm  
Description: Resolution and alignment test patterns.

ID: XARB [AB] Project Name: Arbiter  
Designer: Chuck Thacker  
Bounding box = 2916 x 948 microns, Area = 2.76 sq mm  
Description: None

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Summary of designs from UCB, updated 30-May-80 21:36:13

Allocated 190.00 sq-mm  
Used 91.38 sq-mm  
Remaining 98.62 sq-mm

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ID: AFIFOUCB [DG] Project Name: AFIFO  
Designer: Jim Kleckner  
Bounding box = 4186 x 2980 microns, Area = 12.47 sq mm  
Description: An asynchronous FIFO.

ID: CLSUCB [BH] Project Name: CLS  
Designer: Mark Hofmann, Yiannos Manoli  
Bounding box = 4410 x 3688 microns, Area = 16.26 sq mm  
Description: A Cascadable Linear Sorter, from which one can build (serial) sorting networks which run in linear time and require  $O(n^2)$  hardware.

ID: NIMUCB [AA] Project Name: NIM  
Designer: Lee Melton  
Bounding box = 2256 x 2526 microns, Area = 5.70 sq mm  
Description: A chip to play nim.

ID: RIDAMUCB [DG] Project Name: RIDAM  
Designer: Manolis Katevenis  
Bounding box = 2764 x 2156 microns, Area = 5.96 sq mm  
Description: A Random Insert/Delete/Access Memory.

ID: XbarUCB [DG] Project Name: XBARUCB  
Designer: David J. Hathaway  
Bounding box = 2650 x 2510 microns, Area = 6.65 sq mm  
Description: An 8 by 8 crossbar switch

ID: XFIFOUCB [DG] Project Name: XFIFO  
Designer: Howard A. Landman  
Bounding box = 1920 x 1920 microns, Area = 3.69 sq mm  
Description: A single FIFO cell from the XPORT project with individual access to all control lines.

ID: XHECUCB [AA] Project Name: XHEC  
Designer: Howard A. Landman, Ion Ratiu  
Bounding box = 4160 x 2668 microns, Area = 11.10 sq mm  
Description: 14-bit Hamming Encoder/Corrector from XPORT project. Allows single error correction / double error detection for 9 data bits. Can be used as Hamming bit generator or as corrector for already-encoded word.

ID: XIBUCB [EF] Project Name: Xib  
Designer: H. A. Landman, Ion Ratiu, Joseph Decuir  
Bounding box = 4478 x 6598 microns, Area = 29.55 sq mm  
Description: An integrated input buffer for the X-port project. Preliminary report available from Landman

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Summary of designs from UCLA, updated 30-May-80 21:36:13

Allocated	69.00 sq-mm
Used	30.12 sq-mm
Remaining	38.88 sq-mm

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ID: ADDERISI [BB] Project Name: ADDER  
Designer: Vojin G. Oklobdzija  
Bounding box = 1116 x 600 microns, Area = 0.67 sq mm  
Description: Design of a 4-bit adder with Manchester carry chain.

ID: FIFOISI [BC] Project Name: FIFO  
Designer: Duyet Huu Nguyen  
Bounding box = 1600 x 2594 microns, Area = 4.15 sq mm  
Description: Dual 4-bit, 8-stage, speed-independent fifo.

ID: FOURADDERISI [BC] Project Name: 4X4Adder

Designer: Mohammad Dadseresht

Bounding box = 2386 x 2220 microns, Area = 5.30 sq mm

Description: Using Conditional Sum addition scheme, a multi-operand adder is implemented. Each operand has 4 bits and there are a total of 4 operands. This project is intended to be used as a building block for a multiplier.

ID: IARBISI [BC] Project Name: Interrupt-Arbiter

Designer: Frederick G. Weiss

Bounding box = 1530 x 1228 microns, Area = 1.88 sq mm

Description: AN INTERRUPT ARBITER AFTER THE DESIGN OF MEAD AND SUTHERLAND AT CALTECH.

ID: M16COUNTISI [BB] Project Name: Mod 16 Counter

Designer: Constantine Ananiades

Bounding box = 1376 x 990 microns, Area = 1.36 sq mm

Description: Two-phase dynamic counter with fast carry generation.

ID: OLRADDERISI [BC] Project Name: On-Line Redundant Adder

Designer: Srinivas V. Makam

Bounding box = 1626 x 1828 microns, Area = 2.97 sq mm

Description: Signed-digit Adder for radix=10, redundancy factor=7

ID: OLSORTERISI [BC] Project Name: On-Line Sorter

Designer: Ghobad Karimi

Bounding box = 2124 x 1728 microns, Area = 3.67 sq mm

Description:

1. THE BOUNDING BOX IS  $X1=0, Y1=0$   $X2=2150, Y2=1750$
2. THE NUMBER OF I/O PADS ARE 19
3. THE GLOBAL SCALE FACTOR IS 100/1
4. IT SORTS TWO 4-BIT SERIAL-BIT INPUT WORDS AND PRODUCE A 4-BIT SERIAL-BIT OUTPUT WORD

ID: TESTUCLA [BB] Project Name: Test chip

Designer: R. Conilogue

Bounding box = 730 x 1530 microns, Area = 1.12 sq mm

Description: This chip is a test structure to be used to characterize the device parameters on this MPC run. It is submitted by the Electrical Sciences and Engineering Department at UCLA. This project chip should not be wire-bonded in its package. A probe-card is being prepared for testing this chip.

ID: WEISSUCLA [AD] Project Name: Transient digitizer

Designer: F. Weiss

Bounding box = 3000 x 3000 microns, Area = 9.00 sq mm

Description: A pass-transistor sample and hold array with delay line.

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Summary of designs from UofC, updated 30-May-80 21:36:13

Allocated 65.00 sq-mm  
Used 47.94 sq-mm  
Remaining 17.06 sq-mm

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ID: AMKUofC [CC] Project Name: Automatic Morse Keyer  
Designer: Rod Schlater, Ron Meredith  
Bounding box = 1464 x 1090 microns, Area = 1.60 sq mm  
Description: Forms properly timed and spaced dots and dashes from Automatic Keyer inputs.

ID: DCOMPUofC [CC] Project Name: Data Compressor  
Designer: David Neuder, Noel Zellmer  
Bounding box = 2050 x 1906 microns, Area = 3.91 sq mm  
Description: Compress serial timing data (4-bit words) into a counted-occurrence format

ID: DDRCUofC [CC] Project Name: Distributed Dynamic RAM Controller  
Designer: J. Redman, R. Sud  
Bounding box = 2604 x 1326 microns, Area = 3.45 sq mm  
Description: A SYNCHRONOUS DISTRIBUTED DYNAMIC RAM CONTROLLER.

ID: DIGSYSCLUofC [AH] Project Name: Digital System Clock  
Designer: J. Redfield, K. Mason  
Bounding box = 2536 x 2294 microns, Area = 5.82 sq mm  
Description: A MICROPROCESSOR COMPATIBLE DIGITAL CLOCK.

ID: ELECTBOOKUofC [AG] Project Name: ElectronicBook  
Designer: Jim Murray  
Bounding box = 3618 x 3678 microns, Area = 13.31 sq mm  
Description: ELECTRONIC BOOK. This design is the prototype PLA-based version of the ROM structure to be used in conjunction with an intelligent controller in the implementation of an ELECTRONIC BOOK.

ID: FIFO2UofC [AH] Project Name: FIFO  
Designer: Don Zimmer, Dan Oldfield  
Bounding box = 2000 x 1900 microns, Area = 3.80 sq mm  
Description: Synchronous FIFO

ID: ICPSUofC [CC] Project Name: Interrupt Controller Peripheral Subsystem  
Designer: M. Janes, E. Schade  
Bounding box = 1630 x 958 microns, Area = 1.56 sq mm  
Description: A VECTOR GENERATION CIRCUIT FOR AN INTERRUPT CONTROLLER

ID: OPAMPUofC [AH] Project Name: Op Amp  
Designer: Rich Davis, Wayne Gravelle  
Bounding box = 1650 x 1630 microns, Area = 2.69 sq mm  
Description: Dual NMOS operational amplifier

ID: RAMCUofC [AG] Project Name: RAM Controller  
Designer: Kathy Ader, Jerry Kinsley  
Bounding box = 1590 x 1060 microns, Area = 1.69 sq mm  
Description: 8-stage shift register and R-S flops implementing a dynamic RAM timing generator

ID: SEQCOMPUofC [AG] Project Name: Sequential Comparator  
Designer: Paul Sherwood, Kent Hardage  
Bounding box = 2000 x 1590 microns, Area = 3.18 sq mm  
Description: This circuit performs the type of sequential comparisons commonly found in logic analyzers.

ID: SPGUofC [AG] Project Name: Symmetric Polynomial Generator  
Designer: Richard Lary  
Bounding box = 1856 x 1856 microns, Area = 3.44 sq mm  
Description: Calculates symmetric polynomials in AND and OR via two methods; firstly, for comparison, a modification of the tally circuit is used; secondly, a direct implementation of the recurrence relation defining symmetric polynomials is used.

ID: SPM3BUofC [BD] Project Name: 3-BIT SERIAL/PARALLEL MULTIPLIER  
Designer: K. Black  
Bounding box = 2120 x 1650 microns, Area = 3.50 sq mm  
Description: A THREE BIT SERIAL/PARALLEL MULTIPLIER.

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Summary of designs from UofI, updated 30-May-80 21:36:13

Allocated	97.00 sq-mm
Used	79.09 sq-mm
Remaining	17.91 sq-mm

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ID: ARRDIVUofI [CH] Project Name: Array Divider  
Designer: Larry Hanes, David Yen  
Bounding box = 2616 x 2636 microns, Area = 6.90 sq mm  
Description: FOUR BIT TWOS COMPLEMENT ARRAY DIVIDER

ID: CORRELUofI [EA] Project Name: Correlator  
Designer: Bob Bury, Dan Halperin, Larry Ruane  
Bounding box = 6440 x 2796 microns, Area = 18.01 sq mm  
Description: Correlator chip to be used by the Radio Astronomy Department to process signals from other galaxies.

ID: DELTANETUofI [EA] Project Name: Delta Network  
Designer: Ken Huang, Alex Veidenbaum  
Bounding box = 2700 x 6792 microns, Area = 18.34 sq mm  
Description: Slice of a Delta Network (invented by J. Patel) for Processor-Memory Interconnection. This chip can connect 4 processors to 4 memory modules; data path width is 4 bits. Multiple chips can be used for larger arrays and data path widths.

ID: MULTCHANANUofI [BD] Project Name: Multichannel Analyzer  
Designer: Kent Fuchs, Tim Skitberg  
Bounding box = 3570 x 1726 microns, Area = 6.16 sq mm  
Description: Programmable Multichannel Analyzer to be used for data acquisition in conjunction with particle detectors.

ID: PWMSUofI [BD] Project Name: Programmable Wave form Music Synthesizer  
Designer: Glenn Poole  
Bounding box = 3566 x 3574 microns, Area = 12.74 sq mm  
Description: A 4-channel programmable waveform music synthesizer, using waveforms stored in external RAM.

ID: SYSMULTUofl [AH] Project Name: Systolic Multiplier  
Designer: Bob Montoye, R. Kuhn  
Bounding box = 3570 x 2344 microns, Area = 8.37 sq mm  
Description: Implementation of a 12-bit serial systolic multiplier. Does a multiply in  $O(n)$  area and  $O(n)$  time.

ID: TPMUofl [BD] Project Name: Testable Pipelined Multiplier  
Designer: Joe Luhukay, Bob Montoye  
Bounding box = 2210 x 3878 microns, Area = 8.57 sq mm  
Description: 4 X 4 pipelined array multiplier based on Serra and Cimerra design, and using the pipeline registers for LSSD-like testability.

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Summary of designs from UofR, updated 30-May-80 21:36:13

Allocated	39.00 sq-mm
Used	10.19 sq-mm
Remaining	28.81 sq-mm

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ID: OESUofR [AH] Project Name: Odd Even Sorter  
Designer: Hiro Yuki Watanabe  
Bounding box = 2246 x 1616 microns, Area = 3.63 sq mm  
Description: ODD EVEN SORTER This project sorts 6 words ,8 bits each, using data structure called uniform ladder. It is desiged so that extentions are easily done. The uniform ladder performs an odd-even sort in highly concurrent

ID: RTMULTUofR [AH] Project Name: Real Time Multiplier  
Designer: Gershon Kedem  
Bounding box = 1592 x 1690 microns, Area = 2.69 sq mm  
Description: REAL TIME BIT SERIAL MULTIPLIER: This project implements a multiplier suggested by A. J. Atrubin. (see Knuth Vol2 ,4.3.3-E) .The multiplier is a Chain of finite state machines. This chip is only one finite state machine.

ID: SCDACUofR [AH] Project Name: Switched Capacitor DAC  
Designer: Mark Kahrs  
Bounding box = 2242 x 1722 microns, Area = 3.86 sq mm  
Description: 13 bit switched capacitor DAC

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Summary of designs from USC, updated 30-May-80 21:36:13

Allocated	98.00 sq-mm
Used	80.36 sq-mm
Remaining	17.64 sq-mm

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ID: CELL0USC [AF] Project Name: booth  
Designer: jam,voskanian  
Bounding box = 4990 x 2000 microns, Area = 9.98 sq mm  
description: controller for 10800 alu to carry out booths algorithm

ID: CELL4USC [DF] Project Name: ahead  
Designer: fernandez,mohamad  
Bounding box = 2874 x 2276 microns, Area = 6.54 sq mm  
description: 4-bit adder with carry look ahead

ID: CORDICUSC [CA] Project Name: CORDIC  
Designer: P. Menon, S. Sastry  
Bounding box = 5656 x 4982 microns, Area = 28.18 sq mm  
description: trigonometric function evaluator using the cordic algorithm

ID: FINALUSC [DF] Project Name: 4-bit bitslice microprocessor  
Designer: hayes, sridhar  
Bounding box = 2750 x 3250 microns, Area = 8.94 sq mm  
description: 4-bit bit slice microprocessor

ID: HURAKUSC [DF] Project Name: array  
Designer: rao,hu  
Bounding box = 2818 x 2202 microns, Area = 6.21 sq mm  
description: array processing element for h. t. kungs highly concurrent signal processor

ID: JAGOSZUSC [DF] Project Name: focal  
Designer: jagosz  
Bounding box = 3500 x 2192 microns, Area = 7.67 sq mm  
description: controller for electro-optical focal plane array sensor

ID: MULTUSC [AF] Project Name: Multiplier  
Designer:  
Bounding box = 2736 x 2374 microns, Area = 6.50 sq mm  
description: Bit serial multiplier

ID: SortUSC [AF] Project Name: Self-Sorting-Memory  
Designer: O. Koeneke  
Bounding box = 2010 x 1360 microns, Area = 2.73 sq mm  
description: Memory sorts entries serially but provides random access output.

ID: SRUUSC [AF] Project Name: sru-for-fft  
Designer: Y. Ehrlich  
Bounding box = 1900 x 1900 microns, Area = 3.61 sq mm  
description: shift and rotate unit for fast polynomial transform microprocessor

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Summary of designs from WUSTL, updated 30-May-80 21:36:13  
Allocated 35.00 sq-mm  
Used 21.97 sq-mm  
Remaining 13.03 sq-mm  
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ID: CRSPNTWUSTL [BH] Project Name: Crosspoint switch  
Designer: T. Ravi, W. Thomas  
Bounding box = 1100 x 1626 microns, Area = 1.79 sq mm  
Description: 2x2 2-bit crosspoint switch

ID: MINDISWUSTL [AA] Project Name: Mindis  
Designer: D. Goldfarb  
Bounding box = 1714 x 3376 microns, Area = 5.79 sq mm  
description: Minimum controller for raster display

ID: TAUTESTWUSTL [BH] Project Name: Tau Tester  
Designer: T. Chaney & F. Rosenberger  
Bounding box = 1126 x 1670 microns, Area = 1.88 sq mm  
description: Test circuit for flip-flop resolving time parameter measurement by wafer probing.

ID: THNGLTWUSTL [AA] Project Name: THNGLT  
Designer: T. Chaney  
Bounding box = 1360 x 326 microns, Area = 0.44 sq mm  
Description: FLIP-FLOP TEST CIRCUIT

ID: TMBPLAWUSTL [AA] Project Name: TMBPLA  
Designer: C. Molnar, T. Fang  
Bounding box = 1486 x 1220 microns, Area = 1.81 sq mm  
description: sequence counter and state control for TRIMOSBUS.

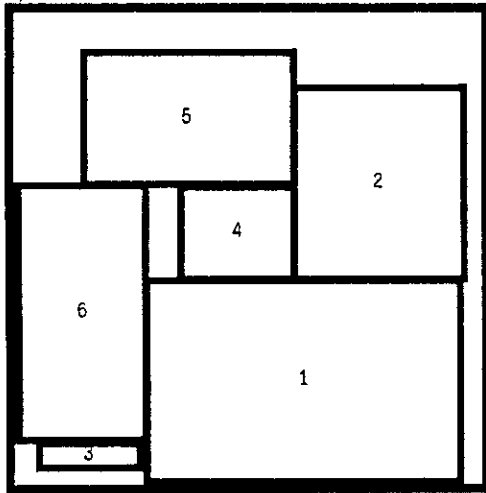
ID: TRIMOSBUSWUSTL [BH] Project Name: TriMosBus-R-S  
Designer: W. Bosch & T. Fang  
Bounding box = 1500 x 1856 microns, Area = 2.78 sq mm  
Description: PART OF CONTROL LOGIC FOR TRIMOSBUS INCLUDING THE RECIEVE AND SEND CONTROL

ID: TRMOBUWUSTL [BH] Project Name: TMBPLW  
Designer: C. Molnar, T. Fang  
Bounding box = 1486 x 1220 microns, Area = 1.81 sq mm  
Description: TRIMOSBUS CONTROL WITH WEAK PULL-DOWN

ID: UNARYDAWUSTL [AA] Project Name: UNARYDA  
Designer: E. Johnson  
Bounding box = 2786 x 1726 microns, Area = 4.81 sq mm  
description: Six bit unary weighted D/A converter with no decoding.

ID: VCOWUSTL [BH] Project Name: VCO  
Designer: J. DeLargy  
Bounding box = 1068 x 796 microns, Area = 0.85 sq mm  
description: A voltage controlled oscillator using voltage control of the gates of depletion mode

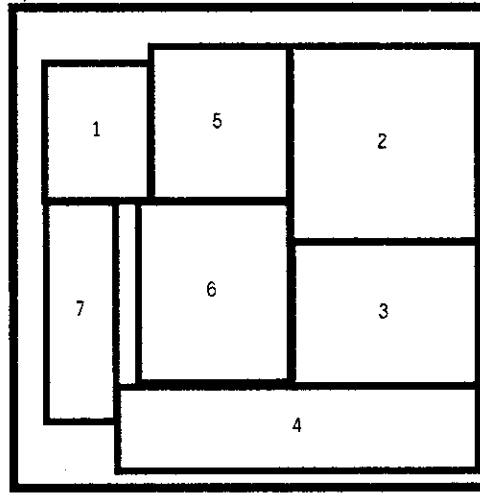
mpc05AA



1 XHEUCB  
2 NIMUCB  
3 THNGLTWUSTL  
4 TMBPLAWUSTL  
5 UNARYDAWUSTL

6 MINDISWUSTL

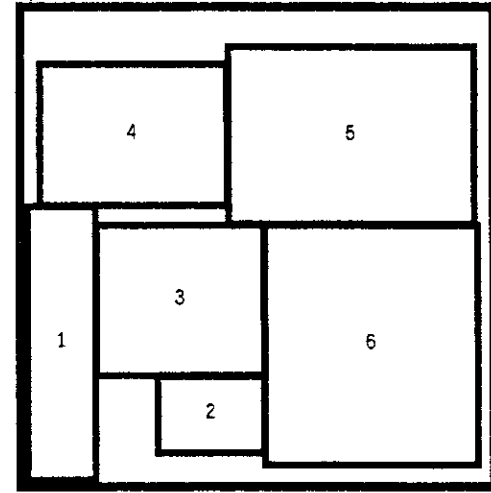
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1 RANDOMSTANFORD  
2 PGSTANFORD  
3 PMULTSTANFORD  
4 CFIRFSSTANFORD  
5 ALU8BSTANFORD

6 PICSTANFORD  
7 XARB

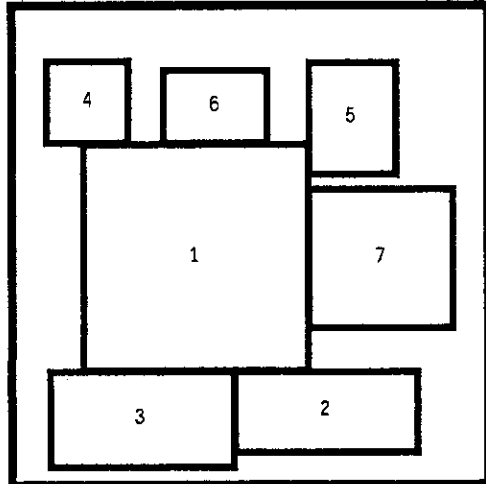
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1 HOORNSCALTECH  
2 DIFETICALTECH  
3 CORBINCALTECH  
4 BYRKETCALTECH  
5 AMCALTECH

6 STDPCALTECH

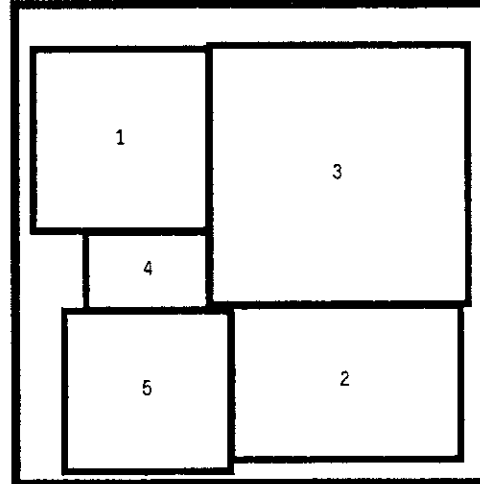
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1 WEISSUCLA  
2 SERIALMULTISI  
3 STGENISI  
4 PADTESTISI  
5 ASTISI

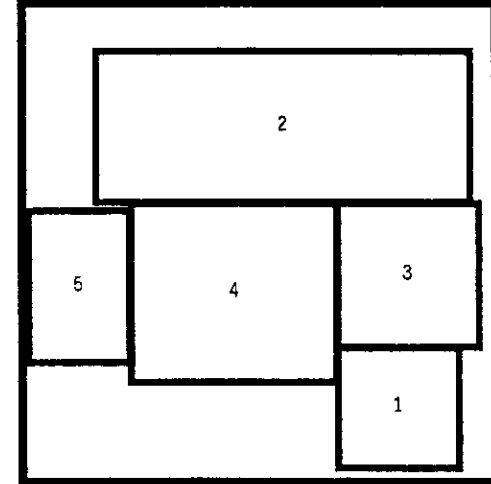
6 DPOMASIB  
7 MORSEISI

mpc05AE



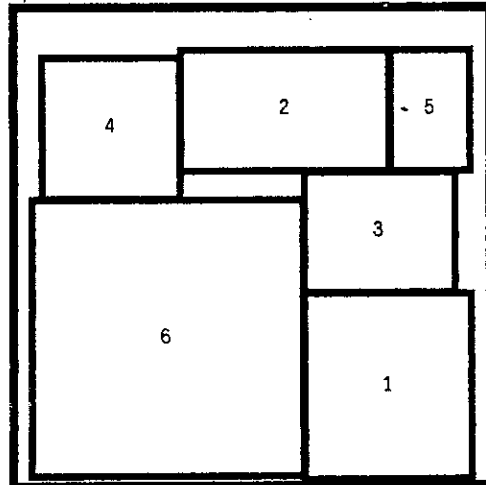
1 POLTEXTCMU  
2 FANCIRCMT  
3 BARSHIFTCMU  
4 SERIALMULTCMU  
5 MAYLEMIT

mpc05AF



1 COMBLOCKUSC  
2 CELLOUSC  
3 SRUUSC  
4 MULTUSC  
5 SortUSC

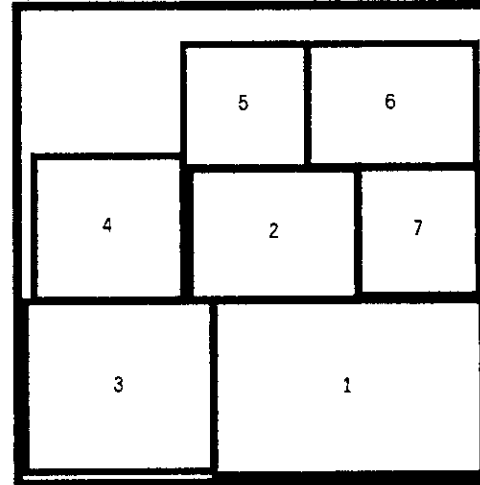
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1 VLFDBBN  
2 STACKBBN  
3 SEQCOMPUofC  
4 SPGUofC  
5 RAMCUofC

6 ELECTBOOKUofC

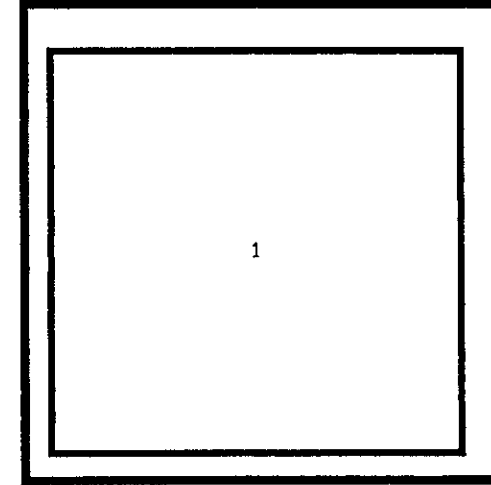
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1 SYSMULTUofI  
2 SCDACUofR  
3 DIGSYCLUofC  
4 FIFOZUofC  
5 OPAMPUofC

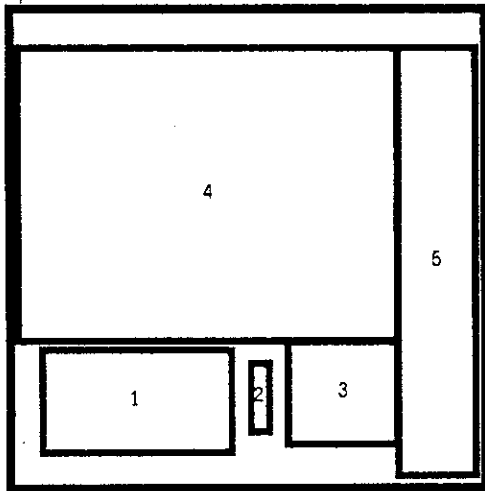
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7 RTMULTUofR

mpc05AI



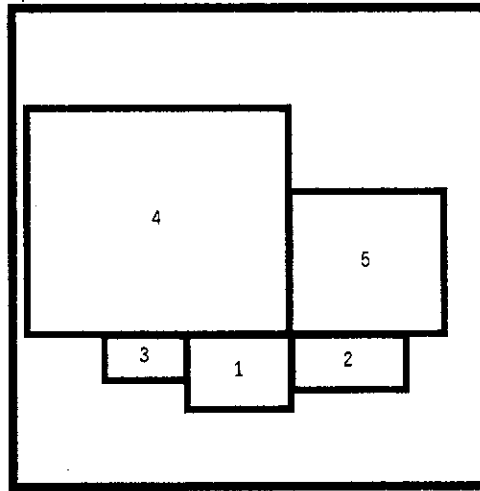
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mpc05BA



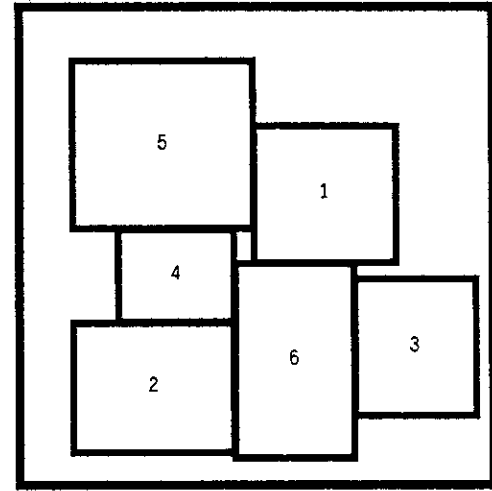
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- 2 EBEAM2MIT
- 3 CGMIT
- 4 BATALIMIT
- 5 VIDBUFCMU

mpc05BB



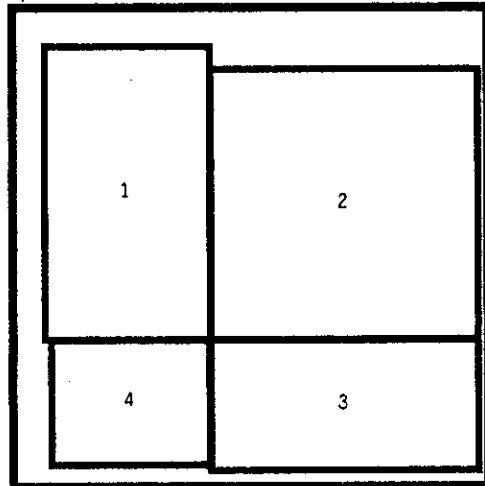
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- 2 TESTUCLA
- 3 ADDERISI
- 4 MEMINTERJPL
- 5 MFLUNDH
- 6 FIFOISI

mpc05BC



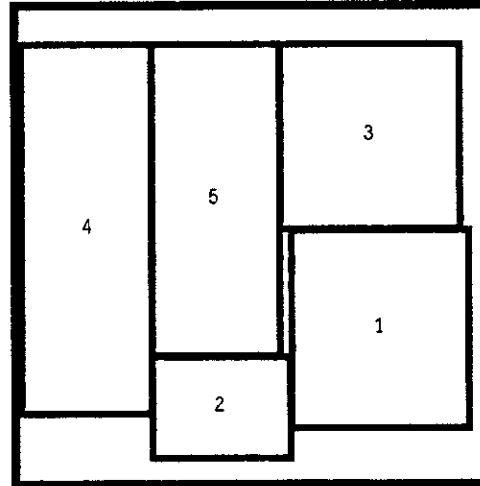
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- 2 OLSORTERISI
- 3 OLRADDERISI
- 4 IARBISI
- 5 FOURADDERISI
- 6 FIFOISI

mpc05BD



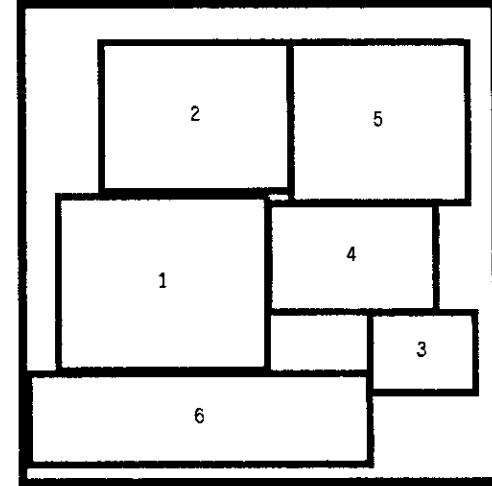
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- 2 PWMSUofI
- 3 MULTCHANANUofI
- 4 SPM3BUofC

mpc05BE



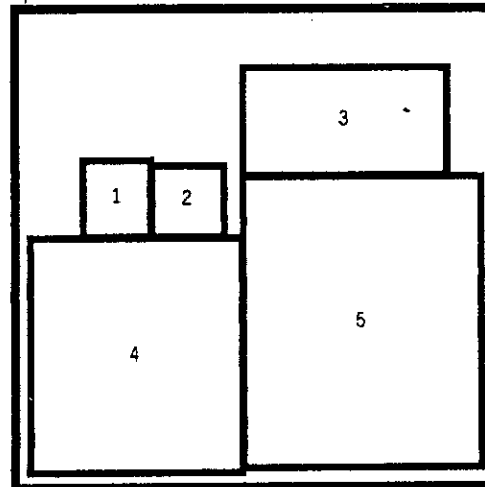
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- 2 PSDSTANFORD
- 3 MYCHIPSTANFORD
- 4 FREDSTANFORD
- 5 DCLOCKSTANFORD

mpc05BF



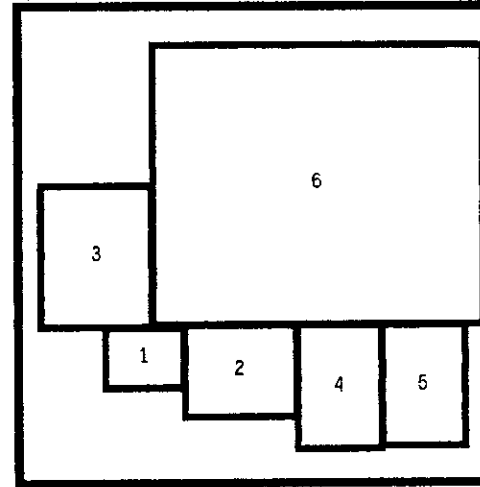
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- 2 SWICALTECH
- 3 STACALTECH
- 4 RDGCALTECH
- 5 STFIFOCALTECH
- 6 KOETHECALTECH

mpc05BG



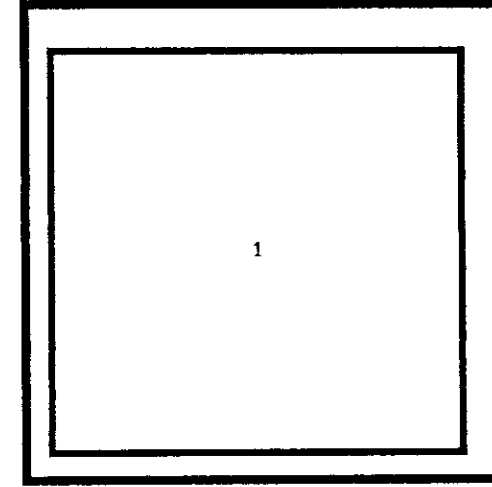
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- 2 DACHIPCALTECH
- 3 STPCALTECH
- 4 PERCIFCALTECH
- 5 OINC2CALTECH

mpc05BH



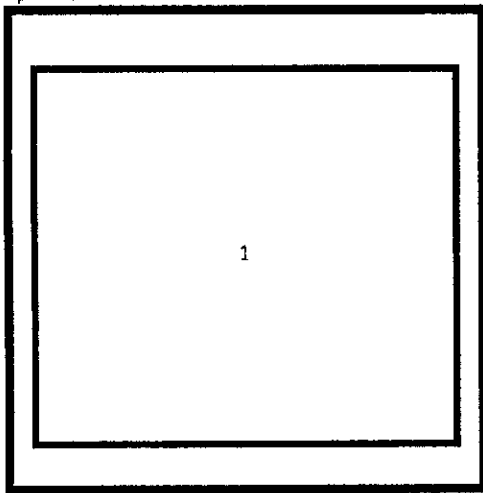
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- 2 TRMOBUWUSTL
- 3 TRIMOSBUSWUSTL
- 4 TAUTESTWUSTL
- 5 CRSPNTWUSTL
- 6 CLSUCB

mpc05BI



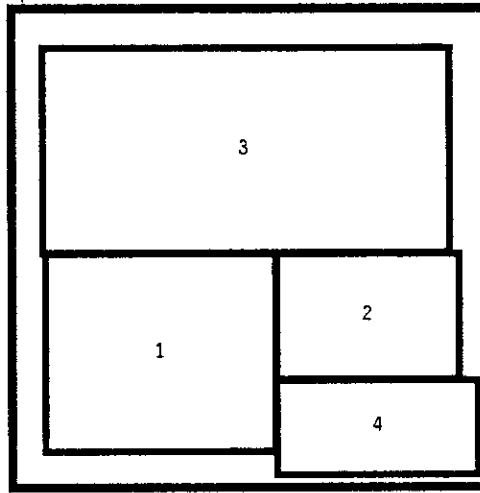
- 1 ALANSPECIAL

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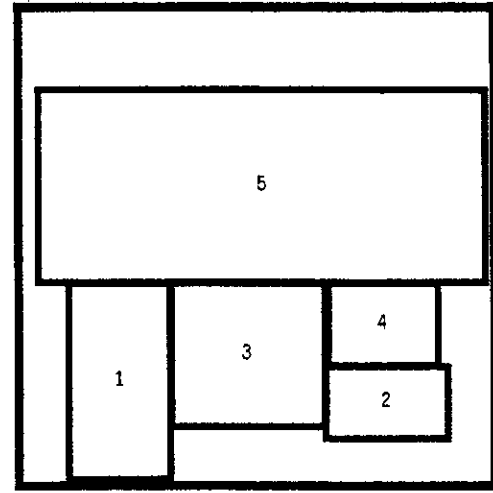
1 CORDICUSC

mpc05CB



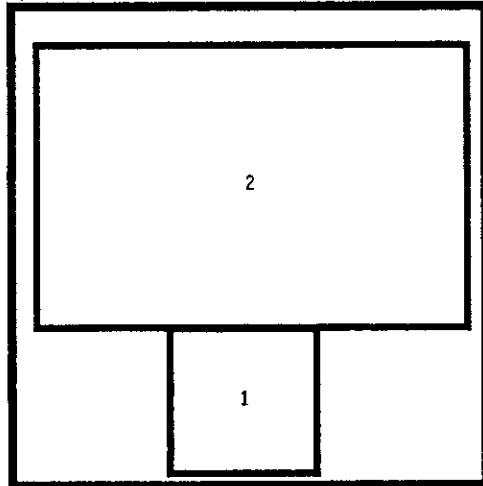
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 3 JEXCALTECH  
 4 CCRTCCALTECH

mpc05CC



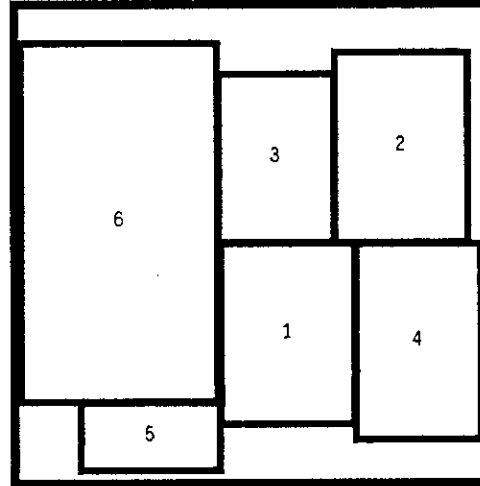
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 2 ICPSUofC  
 3 DCOMPUofC  
 4 AMKUofC  
 5 MultSpec

mpc05CD



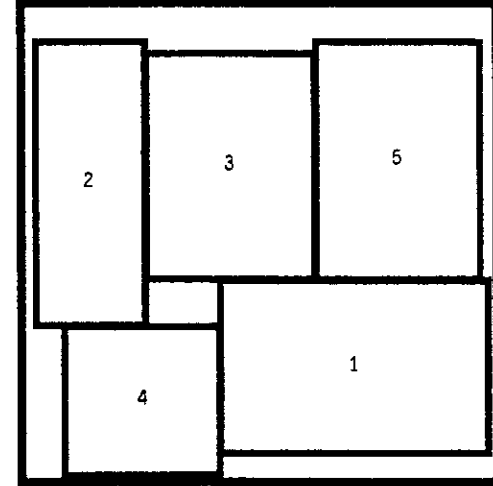
1 RIESMIT  
 2 PORTALMIT

mpc05CE



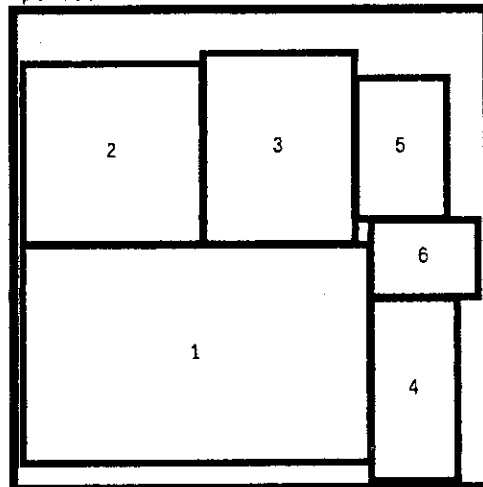
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 3 MULTSTANFORD  
 4 M6800STANFORD  
 5 CCTSTANFORD  
 6 AESTANFORD

mpc05CF



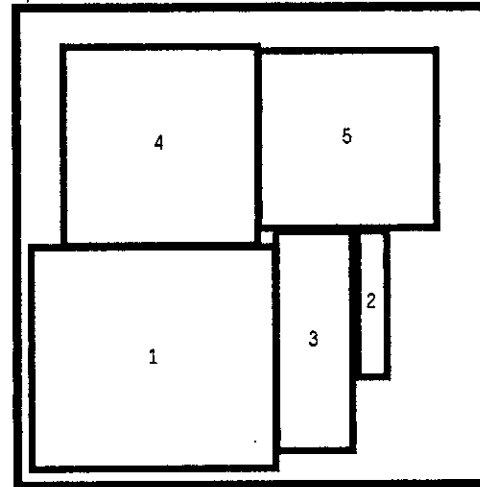
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 4 DRAMCSTANFORD  
 5 ALUTESTSTANFORD

mpc05CG



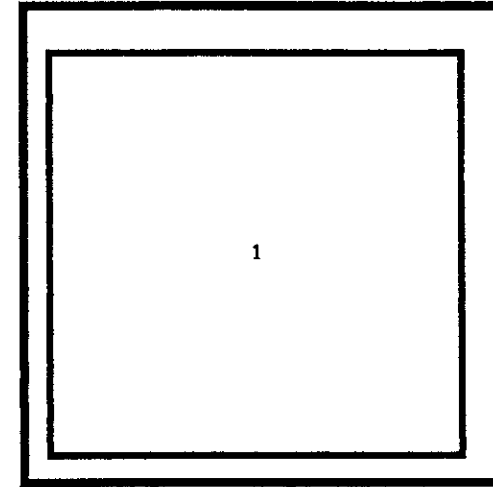
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 5 HLDCCALTECH  
 6 DIFETCALTECH

mpc05CH



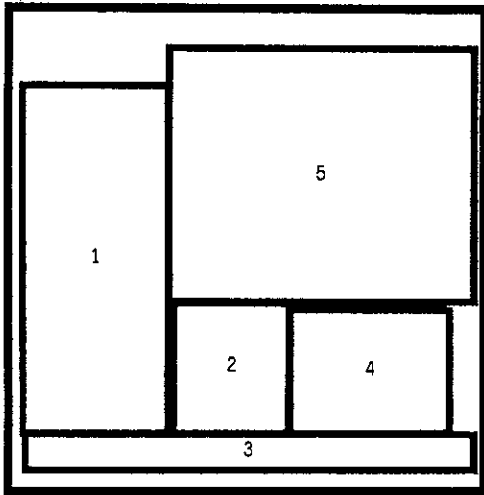
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 2 CETTCMU  
 3 UDCOUNTERCMU  
 4 ARRDIVUofI  
 5 BITARRPROCCMU

mpc05CI



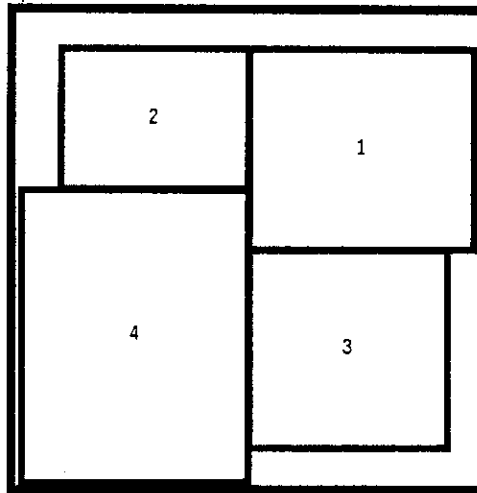
1 ALANSPECIAL

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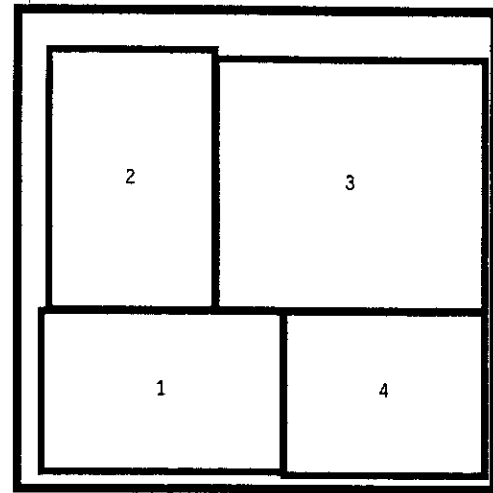
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- 2 RUMPHCALTECH
- 3 MULTIPLIERCALTECH
- 4 FOOBARCALTECH
- 5 DANIELCALTECH

mpc05DB



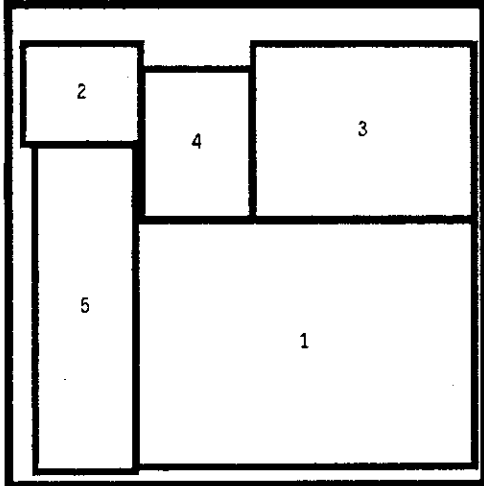
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- 2 CORSICASTANFORD
- 3 BLACKJACKSTANFORD
- 4 AWGSTANFORD

mpc05DC



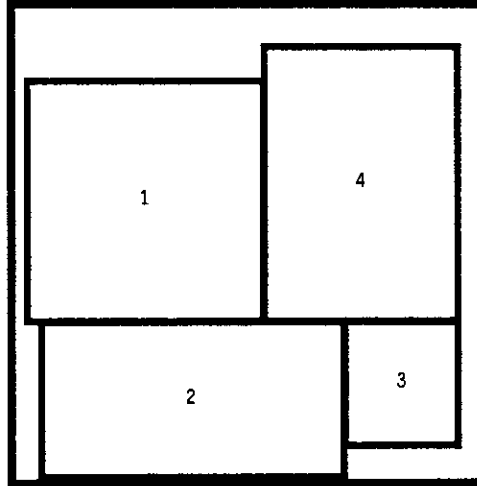
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- 2 KAMCHIPCALTECH
- 3 GR2CALTECH
- 4 JCOLECALTECH

mpc05DD



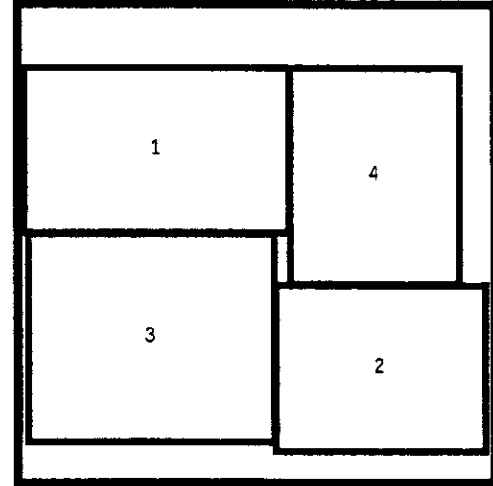
- 1 POTATOSTANFORD
- 2 PFMSTANFORD
- 3 MULTTESTSTANFORD
- 4 EDCCSTANFORD
- 5 ASYNFIFOSTANFORD

mpc05DE



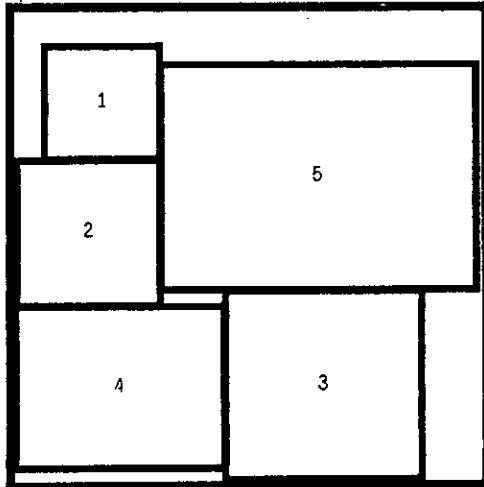
- 1 TCHIPCMU
- 2 PLACMU
- 3 ICSCMU
- 4 DCHIPCMU

mpc05DF



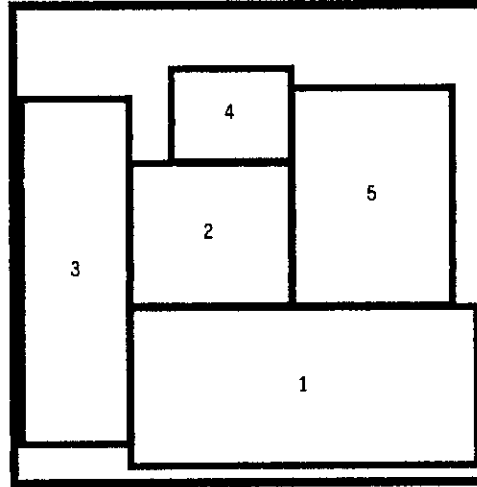
- 1 JAGOSZUSC
- 2 HURAKUSC
- 3 FINALUSC
- 4 CELL4USC

mpc05DG



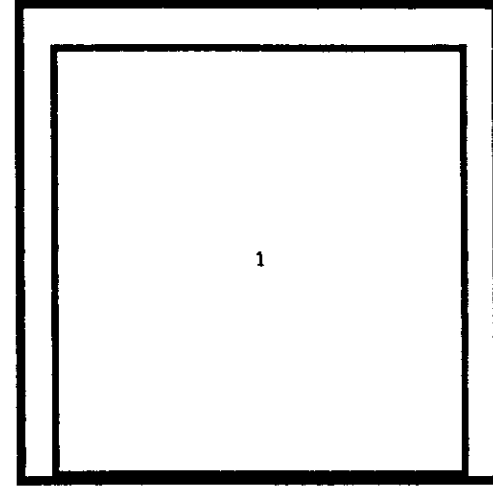
- 1 TALLYSPECIAL
- 2 XFIFOUCB
- 3 XbarUCB
- 4 RIDAMUCB
- 5 AFIFOUCB

mpc05DH



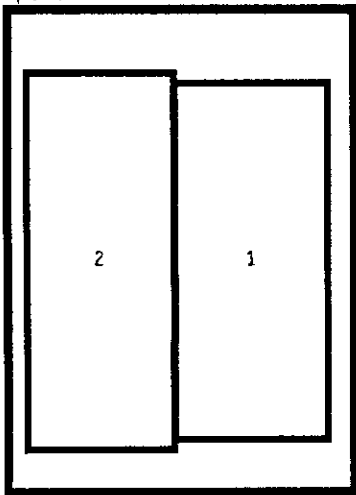
- 1 WOODSBBN
- 2 PSWGBBN
- 3 NOISEBBN
- 4 CRCBBN
- 5 CCITBBN

mpc05DI



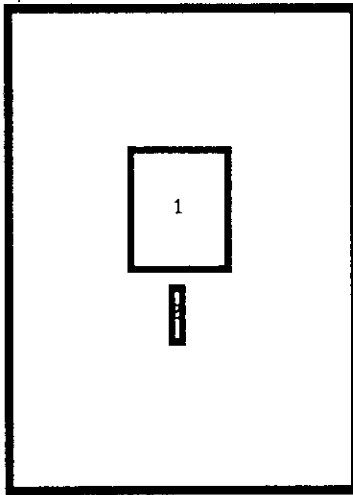
- 1 BILLSPECIAL

mpc05EA



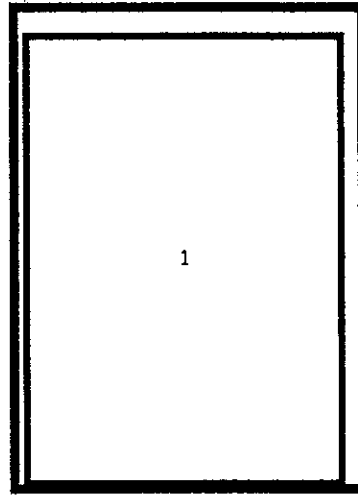
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2 DELTANETUofI

mpc05EB



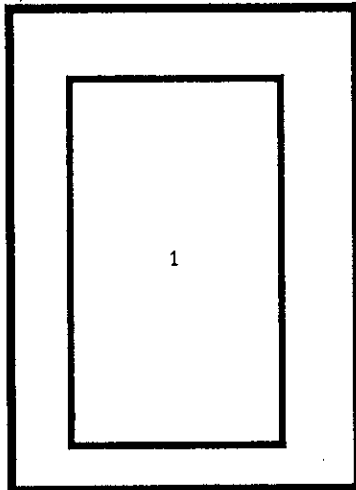
1 PHASEDECSTANFORD  
2 EBEAMMIT

mpc05EC



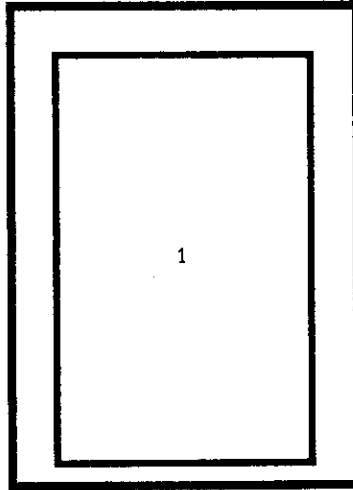
1 RIVESTMIT

mpc05ED



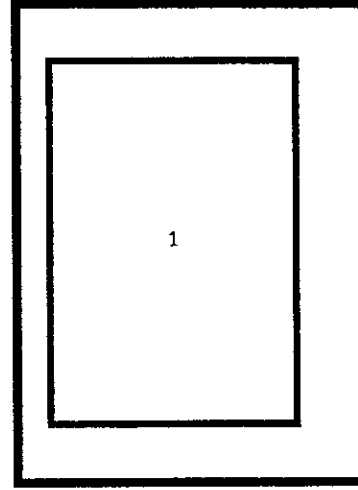
1 SECMIT

mpc05EE



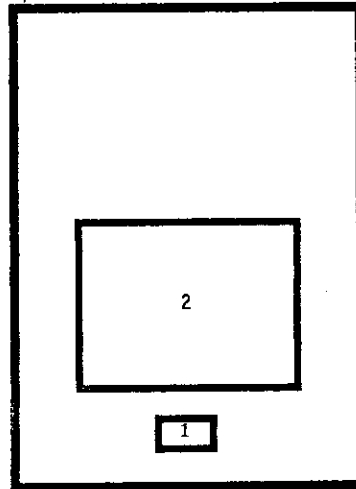
1 TESTCHIPJPL

mpc05EF



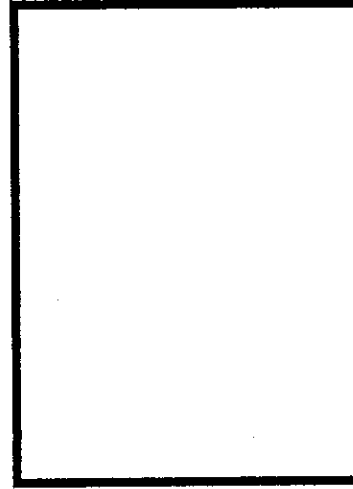
1 XIBUCB

mpc05EY



1 TP580SPECIAL  
2 HPTTESTSPECIAL

mpc05EZ



## 4. Starting Frame Documentation

The following pages describe the structure, function, and use of the various objects in the MPC580 starting frames (a starting frame is the set of all those layout artifacts, not associated with any particular design project, which serve to convey a project chip through maskmaking, wafer fabrication, and electrical testing). Included are the die dimensions and layout, the scribe-line profile, and descriptions of the alignment marks, layer codes, critical dimension testers, etch test patterns, die identification codes, discrete test transistors, ring oscillator, test resistors, contact tester, layer tester, and die code-letters. We used two different starting frames for MPC580. One was used for the first 4 runs which all had the same, relatively small die size. The second was used only on the 5th run which had a relatively large die size to accomodate the larger projects.

### Die Dimensions and Layout

As in the Mead & Conway LSI design philosophy, it is wise to anticipate future miniaturization by parametering the absolute sizes of things. We parameterize the starting frame somewhat by representing the overall die length as L and the overall die height as H.

Overall Die Dimensions: L x H microns

MPC580 dies A,B,C,D:	6350 x 6350 microns	(250 x 250 mils)
MPC580 die E:	6350 x 8686 microns	(250 x 342 mils)

The starting frame dimensions are:

<u>Vertical</u>		<u>Horizontal</u>	
Scribe-Line Profile:	77 microns.	Scribe-Line Profile:	77 microns.
Setback:	21 microns.	Setback:	21 microns.
Universal patterns:	370 microns.	Maximum project:	H - 196 microns.
Setback:	20 microns.	Setback:	21 microns.
Maximum project:	L - 586 microns.	Scribe-Line Profile:	77 microns.
Setback:	21 microns.		
Scribe-Line Profile:	77 microns.		

Maximum Project:

MPC580 dies A,B,C,D:	5764 x 6154 microns	(227 x 242 mils)
MPC580 die E:	5764 x 8490 microns	(227 x 334 mils)

### Scribe-Line Profile.

The scribe-line makes it easier to cut the wafer into dice. The scribe-line profile includes the scribe-line itself and two guard bands of poly and metal. The scribe-line itself is a coincident diffusion, contact cut, and overglass cut, 55, 53, and 40 microns, respectively, to either side of center. This removes all oxide, allowing the wafer saw to cut directly into the silicon wafer. Overlapping the edge of the diffusion by -10 to +8 microns is a band of polysilicon. Seven microns from the diffusion in the scribe-line is a 15-micron-wide band of metal which serves as a visual guide to the saw operator and separates the project area from the saw area.

### Alignment Marks.

Two kinds of alignment marks are provided. In the upper left corner of the die is a square appearing on all layers; this provides a gross alignment indicator. For fine alignment, to its right are a sequence of "Squares" and "Fortresses" as described in Section 6.1 of the Xerox PARC/SSL

Report, *A Guide to LSI Implementation*, 2nd edition, by Hon & Sequin (Sect. 7.1 in 1st edition).

## Layer Codes, Critical Dimension Testers, and Etch Test Patterns (Ells)

Below the alignment marks appears a set of six similar patterns, one for each of the six layers. Each consists of three items: the layer code {DIF, IMP, POL, CUT, MET, or PAD}, two critical-dimension crosses, and a set of L-shaped etch test patterns.

Critical Dimension Testers are two crosses with line widths of two lambda and as follows:

DIF	2 lambda	CUT	2 lambda
IMP	4 lambda	MET	4 lambda
POL	2 lambda	PAD	4 lambda

Etch test patterns (ells) are 26 lambda high. Smaller ells, with one lambda width and spacing, are nested inside the upper right corner of larger ells with two lambda width and spacing. In addition, there is a vertical two-lambda-wide bar down the left side of the pattern to make measurement easier.

Although digital stretching of various layers may be specified for all active devices, no stretching is performed on critical dimension testers and etch test patterns.

## Identification Code

Each die has a unique seven-character identifier, e.g. "MPC05AF". The first three characters "MPC" indicate that this is a Multi-Project Chip. The next two characters indicate the year and month, respectively; i.e., '0' = 1980, '5' = May. The next two characters indicate the wafer and die, respectively. For example, letters "MPC05AF" indicate that this is die type F on wafer type A.

## Discrete Test Transistors

Discrete devices are shown for measurement of dc parameters such as threshold voltages. Figure 1 shows the location within the starting frame and pad connections for the test devices.

Four devices, with sources and gates are bussed together, but having separate drains, are provided. All have four lambda wide by two lambda long channels. There is one device of each of the following types:

- Metal gate, field oxide.
- Poly gate, field oxide.
- Poly gate, thin oxide.
- Poly gate, thin oxide, ion implant (depletion mode),

## Ring Oscillator

The ring oscillator is used to estimate the speed of devices made using this process. It consists of nineteen identical inverters in a circle, and a twentieth as a buffer to drive a line to a standard output pad, where there is more buffering to drive the outside world. Each inverter in the circle is minimum geometry,  $K=4$ . Pulldowns have four lambda wide by two lambda long channels. Pullups have two lambda wide by four lambda long channels. Since the oscillator period  $T$  equals the delay twice around the loop, the inverter pair delay is  $T/n$ , where  $n$  is between 19 and 20 since eighteen of the inverters drive only one similar inverter but the nineteenth drives two.

## Test Resistors

There are two Van Der Pauw structures, one in polysilicon and one in diffusion, with identical geometry as shown in Figure 2. In a Van Der Pauw structure, there are two pads at each end of each resistor to allow separate current feed and voltage sense paths to the layer being tested, so that probe and contact resistance does not introduce error into the measurement. These devices provide a long aspect ratio (266.5 to 280.5 squares, depending on how corners are treated\*) path of

minimum width (two lambda). Because of edge effects, sheet resistivity estimates from these measurements (sheet resistivity = total resistance divided by aspect ratio) are only approximate for other than two lambda wide lines.

\*For further information on paths that go around corners in sheets of resistive material, see D. Vitkovitch, Ed., *Field Analysis, Experimental and Computational Methods*, D. Van Nostrand Co., Ltd., 1966.

### **Visual Identification**

The wafer and die code letters, 370 microns (15 mils) tall, are repeated in the upper right corner of the die, for visual identification. Good eyesight and strong light are needed.

## MPC Starting Frame Test Devices

### Transistors

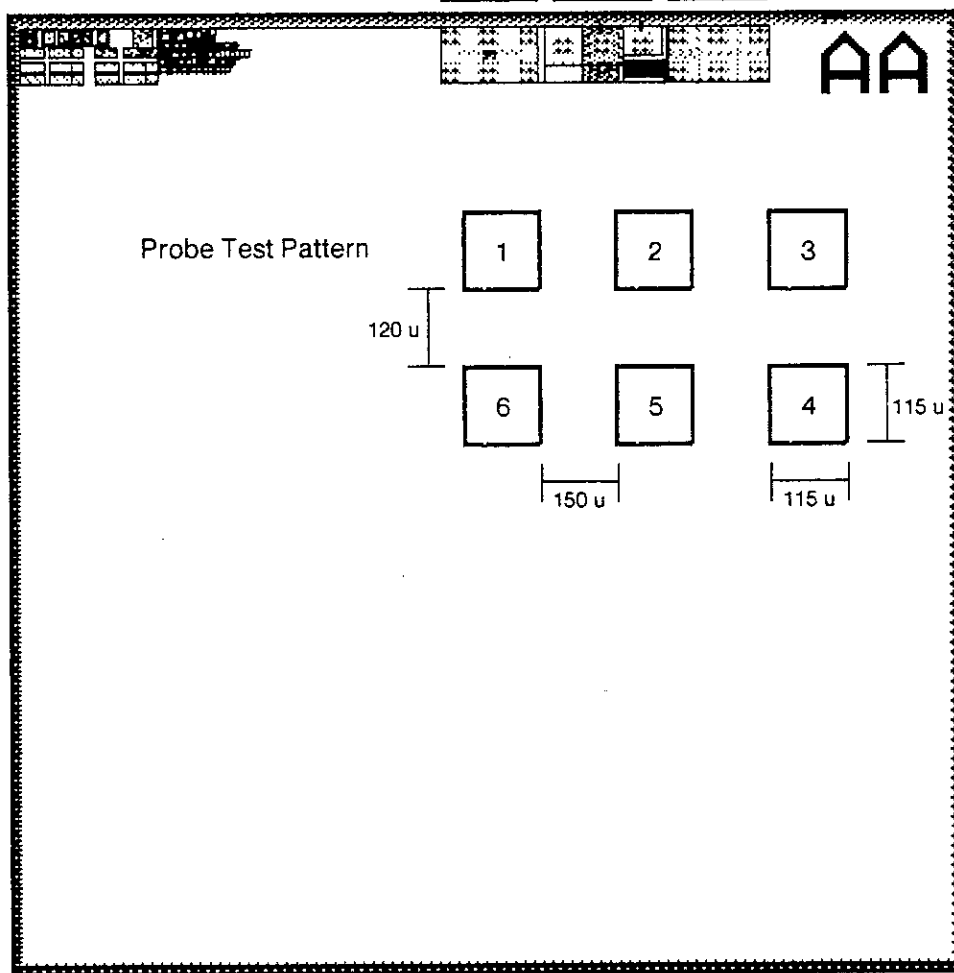
- 1 Drain, metal gate, field oxide
- 2 Drain, poly gate, field oxide
- 3 Drain, enhancement mode
- 4 Drain, depletion mode
- 5 Source (common)
- 6 Gate (common)

### Ring Oscillator

- 1 Scribe line
- 2 Scribe line
- 3 Scribe line
- 4 Vdd (+5v)
- 5 Output
- 6 Ground

### Resistors

- 1 Poly end
- 2 Poly end
- 3 Center
- 4 Center
- 5 Diffusion end
- 6 Diffusion end



## 5. Electrical & Process Measurements

This section provides the results of electrical measurements made at the Hewlett-Packard Integrated Circuit Processing Laboratory using the MPC580 starting frame test structures. Included are the ring oscillator frequency, the various threshold voltages, certain electrical parameters, and basic information about the process, such as oxide thicknesses.

The transit time,  $\tau$ , of minimum-sized transistors can be derived from this information, and then used by designers to estimate the maximum clock frequencies for their projects. The nineteen-stage ring oscillator "rings" at  $\sim ?$  MHz (at  $V_{DD} = 5v$ ). Thus the inverter-pair-delay in the oscillator equals ? ns (see Section 4, Starting Frame Documentation). Let's assume that the effective fanout,  $f$ , including parasitics is approximately equal to 2. The inverter-pair-delay =  $f(k+1)\tau = ?$  ns. Therefore, we find that the transit time  $\tau$  is approximately ? ns.

## 6. Request for Feedback and Further Plans

### Feedback about Testing

We are very interested in knowing whether your projects worked. Even if they didn't work, and you know why, we'd like to know about that. Let me encourage you to send test results either via network mail to MPC580 at PARC-MAXC or via US mail to:

Ted Strollo  
c/o Xerox PARC  
3333 Coyote Hill Rd  
Palo Alto, CA 94304

### Submissions of Cells to the Library

We encourage you to submit clever new cells you would like to share via the library. Please send information about such cells to Ted Strollo per the mechanisms suggested above. I will need the CIF file of your cell (You can simply send me that in a message) as well as a complete description of what it does. Please send a check plot too.

### Plans for Packaging More Chips

Since we have only limited packaging capabilities, we are distributing only one packaged chip per project for most of the projects. In some cases, where we know that projects will undergo immediate functional testing, we are distributing two or three packaged chips per project.

There will be a need for further packaging. Probably the largest demand for this additional packaging will be for projects having multiple designers, so each designer can have a copy. We are shipping a moderate number of unpackaged chips to each coordinator, and coordinators may be able to make local arrangements for the packaging of these additional chips.

So, if you'd like to get hold of more packaged chips, talk to your project coordinators. They may be able to make the local arrangements, or they may relay your request on to us. We'll expedite the packaging of additional chips for those who plan to do some serious functional testing, especially for the larger projects (if your project has a very large area, you may need to test several copies of it, in order to separate possible design errors from possible fabrication defects).

### How to obtain Chip Photographs

Melgar Photographers is making photographs of the individual die-types. A separate order blank is included with this document for you to order photographs direct from the photographer.

## ORDER FORM FOR MPC580 PHOTOGRAPHS:

To order photos of MPC580 Dies and/or individual Projects, complete this order form and mail to:

**Melgar Photographers, 2971 Corvin Drive, Santa Clara, CA 95051.**

Please make checks payable to *Melgar Photographers*. If you have any questions, contact Melgar at (408) 733-4500.

### *Unit Prices:*

Size	BW	Color
5" x 7"	\$2.25	\$3.50
8" x 10"	3.00	6.00
11" x 14"	8.00	12.00
16" x 20"	12.00	25.00
20" x 24"	15.00	30.00

### *Customer Address:*

Name: _____
Address: _____
City: _____
State: _____ ZIP: _____
Phone: _____

**Full die Photographs:** (Please print Project ID carefully; an example ID: RIVESTMIT)

QTY	Size	Color or BW	MPC580 Project ID	Unit Price	Total Price

**Individual Project Enlargements:** (Please print Project ID carefully; an example ID: RIVESTMIT)

QTY	Size	Color or BW	MPC580 Project ID	Unit Price	Total Price

Subtotal: \_\_\_\_\_

+6.5% Sales Tax if CA order: \_\_\_\_\_

+2.50 for postage and handling: \_\_\_\_\_

Final Total: \_\_\_\_\_

2.50