Departement of Physics and Measurement Technology

A CMOS DESIGN MANUAL

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Contents:

1. Introduction
2. The CMOS principle
3. Some simple CMOS circuits
4. The metal gate CMOS process and design rules
5. Stick diagrams
6. CMOS logic circuitry
7. Electrical constraints
8. Design methology
9. Some process parameters
10. The silicon gate CMOS process and design rules.

1. Introduction.

This short design manual is aimed to introduce a student to CMOS technology so that he can design simple MOS circuits in a multiple project chip enviroment. The manual treat only CMOS technology.

2. The CMOS principle.

CMOS technology is based on two devices, n-channel and p-channel MOS-transistors. The use of this complementary pair of devices gives CMOS digital circuits with some unique properties. They will be highly symmetric (with respect to zero and one), they will have large signal margins (the zeros and ones will be very distinct) and they will use very little power (power is used only for transitions). These properties makes CMOS a very attractive technology for VLSI circuits in the future.

In fig. 1 we show shematic pictures and current voltage characteristics of the two transistor types. The current voltage characteristic for an n-channel transistor can be written:

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ID = KP*(W/L)*< u(VG-VT) - u(VG-VT-VD) > ,

u(X) = <(X + ABS(X))/2>**2
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where KP is a constant, W/L is the width to length ratio of the transistor, VG is the gate voltage, VT is the threshold voltage of the transistor (a constant) and VD is the drain voltage. The characteristic of the p-channel device is obtained by changing sign of ID and all voltages. A very simple view is to assume that an n-channel device is open for zero gate-source voltage and shorted for a high gate-source voltage and that a p-channel device also is open for zero gate-source voltage but shorted for a high negative voltage.

The principle of the CMOS digital circuit family is clearly seen in fig. 2. When the input voltage VIN is zero (VSS) the n-channel device is open and the p-device is shorted. This makes the output voltage high, VOUT = VDD. Similarly VIN = VDD makes the output voltage low, VOUT = VSS. The operation is completely symmetric with respect to VSS and VDD. The output signal is locked to either VSS or VDD. Note also that in neither state is there a current path from VDD to VSS, thus the circuit use no static power. Finally note that the substrate of the n-channel device is connected to VSS and the substrate of the p-channel device to VDD. The two substrates may therefore be used as VSS and VDD supply lines.

How do we find a practical way to fabricate the CMOS circuits? In fig. 3 we show the real structure of a silicon crystal with a CMOS inverter integrated in it. We can note that the p-channel MOS

transistor is made directly in the n-type silicon wafer. The n-channel device is made in a special p-well, formed by diffusing in p-dopant into the wafer in selected areas. The p-well and the n-wafer makes up a pn-diode. However as this diode always is backbiased (as the n-substrate is connected to VDD and the p-well to VSS) it will not affect our circuit at all.

3. Some simple CMOS circuits.

The simplest CMOS circuit is the inverter circuit already shown (fig. 2). This circuit can easily be extended to NOR and NAND gates, see fig. 4. In the case of the NOR gate VOUT=0 if any of the inputs are high (shorting the output to VSS) and VOUT=VDD only if both inputs are low (shorting the output to VDD). As in the case of the inverter no current flows in either state. Comparing with the NAND gate again demonstrate the symmetry of CMOS. The NAND gate is obtained if the NOR gate is put upside down or if the logic notation is changed from positive to negative logic.

Another circuit example is the transmission gate (pass gate) shown in fig. 5. The pass gate is used as a switch, controlled by P. Its simplicity and its property to be bidirectional makes it a very useful device.

4. The metal gate CMOS process and design rules.

As different processes have different geometry and as geometry becomes smaller with time it is convenient to relate all measures to a unit size, LAMBDA. LAMBDA can for example be the largest mask error which can occur in the process.

Let us take a closer look upon the fabrication process for metal gate CMOS circuits. In fig. 6 we show the whole fabrication process in steps corresponding to the different masks used. We show only the process for the n-channel transistor. The p-transistor fabrication is completely analogous, one just exchanges n and p diffusions and deletes the p-well and the guard.

The first process is to use an oxide mask to define the p-well area. The right hand part of fig. 6 shows the mask. The p-well is diffused into the silicon wafer through the opening in the oxide. As this diffusion is rather deep one must remember that it also diffuses under the oxide edge as shown in the figure. We will return to this.

Next step is the p-diffusion which is used for source and drain in p-transistors and for guard bands around n-transistors. Guard bands are used in the actual process to avoid so called latch-up (to be discussed in section 7). The p-diffusion is not so deep, but gives anyway some underdiffusion near the oxide edge, d. Assuming d to be less than LAMBDA allows us to put diffusions as close as 4 units of

LAMBDA without risk for shorts. This is thus the first design rule. Furthermore we will not allow the diffusion to be narrower than 4 units. We may also understand the p-well mask now. By always putting the p-well mask edge 3 units inside the outside edge of the p-guard band, its underdiffusion will be masked by the guard. Then we do not need to consider this underdiffusion any further in our design work.

Next step concerns the n-diffusion for drain and source of our n-transistor. Again, we have a small underdiffusion , d. This mask sets the important channel length of the transistor, L. As d normally is of the order of half the LAMBDA unit we may allow the masked value of L to be 3 units. The real L then becomes 3LAMBDA - 2d. In some cases it is of interest to contact the transistor source with its guard band or its substrate. This is done by putting the two diffusions together and placing a metal contact on top. Note that the two diffusions can not be contacted directly. Without the metal short we will get a pn-diode.

We will now open holes in the field oxide for thin oxide areas. As shown in fig. 6 openings are formed both over transistor gate areas and over contact cut areas. In the transistor gate area is the field oxide opening overlapping the diffusions by 2 units. It is very important that the gate metal control the channel all the way to the n-diffusion edges. It must also control the whole thin oxide part of the gate area, thus it must overlap the field oxide edge 1 LAMBDA at the transistor edge. The field oxide opening around the contact cut shall overlap the coming contact cut by 1 unit. This is to make the contact opening easier to etch.

The contact cuts are now formed. The important point is to have the opening large enough to give reliable contacts. We have chosen a minimum opening of 4 x 4 units. Furthermore the opening must be at least 2 units inside a diffusion edge to avoid any shorts to substrate.

The final mask is the metal mask. For the metal we will use the following rules. Minimum width 4 units, minimum separation 3 units, minimum overlap over source and drain diffusions 1 unit and minimum overlap over field oxide edge and at transistor edges 1 unit. Over a contact cut we are satisfied by a zero overlap.

The complete design rules are given in Table 1 and are demonstrated in fig. 7.

In some cases a more complete set of guard bands are used in order to prevent surface leakage currents. This is often used when the CMOS circuit is to be operated at higher voltages, e.g. 15 V. In such a case each transistor and each diffusion is surrounded by a guard band with opposite doping. Also, the gate metal is always arranged so that it controls all area between a transistor gate edge and the nearest guard band. The additional design rules for a completely guarded CMOS process are demonstrated in Table 2 and fig. 8.