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VLSI Training-Enhancing the Silicon Broker/Foundry Concept

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SUMMARY The rapidly increasing complexity of silicon chips coupled with a corresponding increase of chip designers and potential designers has made the concepts of the silicon foundry and silicon broker a reality over the past two years. These businesses, configured to ease the coupling between chip designs and the backend services required to implement them into silicon, have done a good job in allowing the designer to concentrate on the functional portion of the digital chip. Part of the role of the foundry/broker is the teaching of good VLSI design techniques to perspective customers, generally along the lines of the Mead-Conway structured methodology. Besides generating a larger potential customer base, the training course provides additional benefits in the areas of verification of CAD software and hardware tools and standardizing interfaces between the designer and the foundry. Each of these points will be discussed in this paper.

1. INTRODUCTION

The basic concepts of the Carver Mead-Lynn Conway methodology of design are familiar to virtually anyone who has interest in the design of LSI/VLSI silicon chips. Outlined in their textbook (Mead and Conway, 1980), this design philosophy addresses the problem of handling the complexity of management of design for chips containing, even now, hundreds of thousands of transistors. Developed in the engineering universities, Mead-Conway design courses spread to various electronics companies for in-house training of VLSI design (Lipman, 1981) and then to the newly formed silicon foundries and brokers.

Whereas the role of the silicon foundry is to perform one or more of the backend services required after a design is completed, the silicon broker acts as an interface between the designer and the mask making, processing, packaging and testing operations. In other words, the broker links the designer to the foundry services. This relieves the designer of a complex and often frustrating supervisory task that detracts from the design of the actual functional chip.

One of the roles adopted by the broker and/or foundry is the training of LSI/VLSI designers. Through the development of various on- and off-site courses, the designer learns the techniques involved in good silicon chip design and development. By making the actual design of a chip chosen by the student a part of many of the courses being offered, the designer gains the actual "hands-on" experience that is necessary in the education of top-level IC designers.

2. COURSE DESCRIPTION

Each of the courses offered by the broker or foundry have two common points. First, all center around the Mead-Conway design methodology which advocates splitting the functional chip design from the tasks concerned with processing, packaging and the other backend services. This approach takes the view that the chip is a self-contained system and that this idea should be foremost in design. Second, the use of state-of-the-art CAD software and hardware tools is taught during the courses for chip simulation, design and verification. Emphasis is given to the notion that the silicon system's behavioral and physical properties must be considered concurrently during the design cycle.

There are two general types of basic design courses. The first is spread over a ten week time period with three hours of formal lecture a week. During the first five weeks of the course, homework and reading assignments are given. Students do their chip design during the last five weeks, a task which takes up about 16-20 hours a week in addition to the lecture time.

The second type of general course, as taught by VLSI Technology, Inc. of Santa Clara, California, is four weeks in length, five days a week. The first week is devoted to lectures and homework assignments. The lectures are comprised of live instruction and video tapes of a number of experts in the VLSI design field. The following three weeks of the course are devoted almost entirely to work on an actual IC design project. This type of class is of particular benefit to those interested individuals who are beyond normal commuting distances to the sponsoring company.

Both courses include the implementation of the chip designs onto silicon by the organization doing the training. This phase of the class is marked by fast turnaround of the design, typically under six weeks from design completion to packaged chips.

In addition to the basic full design course, other options offered by the broker or foundry include short (two or three day) seminars on emerging VLSI technologies, such as CMOS, one week "train-the-trainer" courses and one- to two-week seminars at the customer's site.

At this time, the short seminars are aimed at those people who have taken a Mead-Conway design course using NMOS as a design vehicle and now wish to move into the design of chips in other technologies. Presently, bulk CMOS is an ideal candidate and a number of two day CMOS seminars have been taught by the author.

Training-the-trainer courses allow individuals to return to their own organizations and impart the design methodology to colleagues. The broker and foundry hence leverage off the training effort and further increase the number of chip designers. In addition, these people are made more aware of the advantages of having designs implemented quickly and inexpensively via a foundry operation.

Intensive training courses at a customer's site permit the customer to educate a large number of people simultaneously for a minimum of expenditures. The content of such a course is also flexible to permit configuration to a particular customer's requirements.

3. LAMBDA DESIGN RULES

The Mead-Conway design approach makes use of a simplified set of geometric design rules based on a scalable quantity called lambda. The lambda design rule set represents the resolution of a typical photolithographic step used in the processing of a silicon wafer (Lyon, 1981). In their textbook, Mead and Conway define a set of design rules of NMOS that is an integral part of most of the Mead-Conway courses taught today. A similar set has been developed for a bulk, oxide-isolated, p-well, CMOS process (Lipman, 1981) and is given in Figure 1.

The use of a lambda design rule set results in a number of advantages to both the designer and the foundry/broker:

a. Ease of understanding by the designer. The typical 30-40 page set of design rules is condensed to about two pages.

b. The designer is now able to focus on the functional design of the chip. Factors having to do with backend services, such as mask making, processing and packaging, are tied to all designs in a given technology and are hence addressed by the broker and foundry.

c. With some notable exceptions (such as pads), these rules allow the design to reasonably track scaling changes in the process since lambda is scalable. Prebiasing (i.e., bloating or shrinking) of individual mask layers is of no concern to the designer; it is handled by the broker or foundry.

d. The generality of the lambda design rule set allows for the multisourcing of process foundries when necessary.

e. The definition of a lambda design rule set is an important factor in the consideration that the foundry should be driven by the design, not the other way around.

4. DESIGN IMPLEMENTATION VIA THE MULTIPLE PROJECT CONCEPT

When student designs are completed at the end of a course, it is necessary to implement the design in silicon as quickly as possible so that the packaged chips can be returned to the students for detailed functional evaluation. Two techniques have been developed for doing this, both utilizing the concept of multiple designs sharing a common photomask set and common wafers.

4.1 Multiproject Chips (MPC)

This is the technique developed early in the Mead-Conway course and described in (Hon and Sequin, 1980). A common die size is defined (usually around 250 mils on a side) and the project chips are packed into as few a die as possible, ideally with the help of software implementing some packing algorithm. The various die are then arranged on a common wafer set with photoplates written at 1X using an ebeam machine. An example of an MPC chip is shown in Figure 2.

A major advantage of this approach is that all the projects on a wafer share the cost of the photoplate fabrication and the wafer processing. In addition, a test structure "strip" may be defined for each die and each strip can be probed automatically to decide whether or not an individual die should be packaged and bonded. Detailed process parameters may still be obtained through the use of process control monitor "drop-ins" on each wafer. A disadvantage of this procedure is that only one project on a die is bonded in a package with the resultant waste of the remaining silicon area on that particular chip.

4.2 Multiproject Wafers (MPW)

In this technique, the project designs are merged into a common wafer set with each project within its own scribe line boundary. The merging may be accomplished by software which takes into account chip yield (as a function of size) on both a global (wafer run) and local (chip position of the wafer) basis. Designs are placed such that each has the same probability of being free of process defects, nominally >.99. An example of a MPW is given in Figure 3.

The cost advantage is similar to the MPC wafers but the quantity of unused silicon is now substantially decreased. In addition, a designer is assured of the security of his design since no one else will receive his chip, albeit unbonded, in their package.

6. ADVANTAGES OF FOUNDRY/BROKER VLSI DESIGN TRAINING

A major goal of the VLSI design classes developed by a foundry or broker operation is the creation of additional chip designers that will then utilize the services of the training organization. The student learns a good, structured system approach to the design of an LSI/VLSI silicon chip in a relatively short time frame. This does not mean that the student has become an expert, or even a very good IC designer. This can be accomplished only through experience. What is gained is the establishment of a proper design foundation which is immediately applied by the student in the class projects and later built upon in the development of custom chips in an industrial environment. In addition, other benefits are accrued by both the designer and the foundry/broker.

A variety of CAD tools are provided by the trainer for chip layout, analysis, simulation and verification. These software and hardware packages are either obtained from an outside source (university and/or industrial vendor) or developed in-house by the foundry or broker. In either case, the course scenario provides an excellent opportunity for the evaluation of such tools by the students in an actual working environment. Furthermore, the students get a chance to gain experience with

these CAD tools before making a decision as to whether or not their organization should purchase them for its own use.

Another advantage is the opportunity for the creation of interface standards to the backend services, i.e., masks, processing, packaging and testing, by a joint effort between the foundry/ broker and the designer. Such standardization is sorely needed as anyone who has just gone through the chip implementation phase of their first design will readily attest to. Areas of particular importance include test structures, both parametric and higher level cell, for the evaluation of foundry processing, commonality of communications between designer and foundry, and the creation of high level library cells for the newer technologies, such as CMOS.

7. CONCLUSIONS

In summary, the undertaking of VLSI training courses by a foundry or broker operation can result in substantial benefits to both the training organization and the student. More designers are created to address the rapidly increasing number of custom LSI/VLSI chip designs. CAD software, which is presently inadequate for the complexity of designs being undertaken, is developed, evaluated and modified in a fast turnaround design environment. Students are provided a good structured design foundation which is then applicable to subsequent chip designs of increasing complexity. Finally, the opportunity exists for the creation of interface standards between the designers and foundries which result in advantages for the entire VLSI community.

8. REFERENCES

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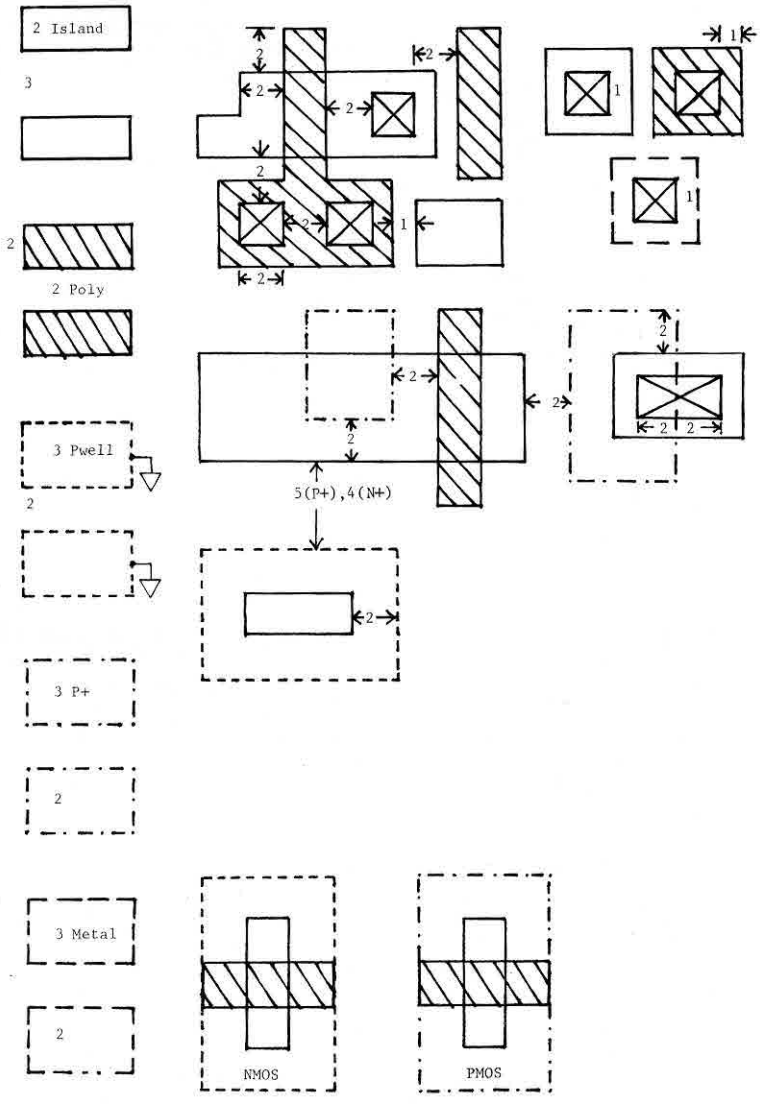

Figure 1 Lambda Design Rule Set for a Bulk CMOS Process

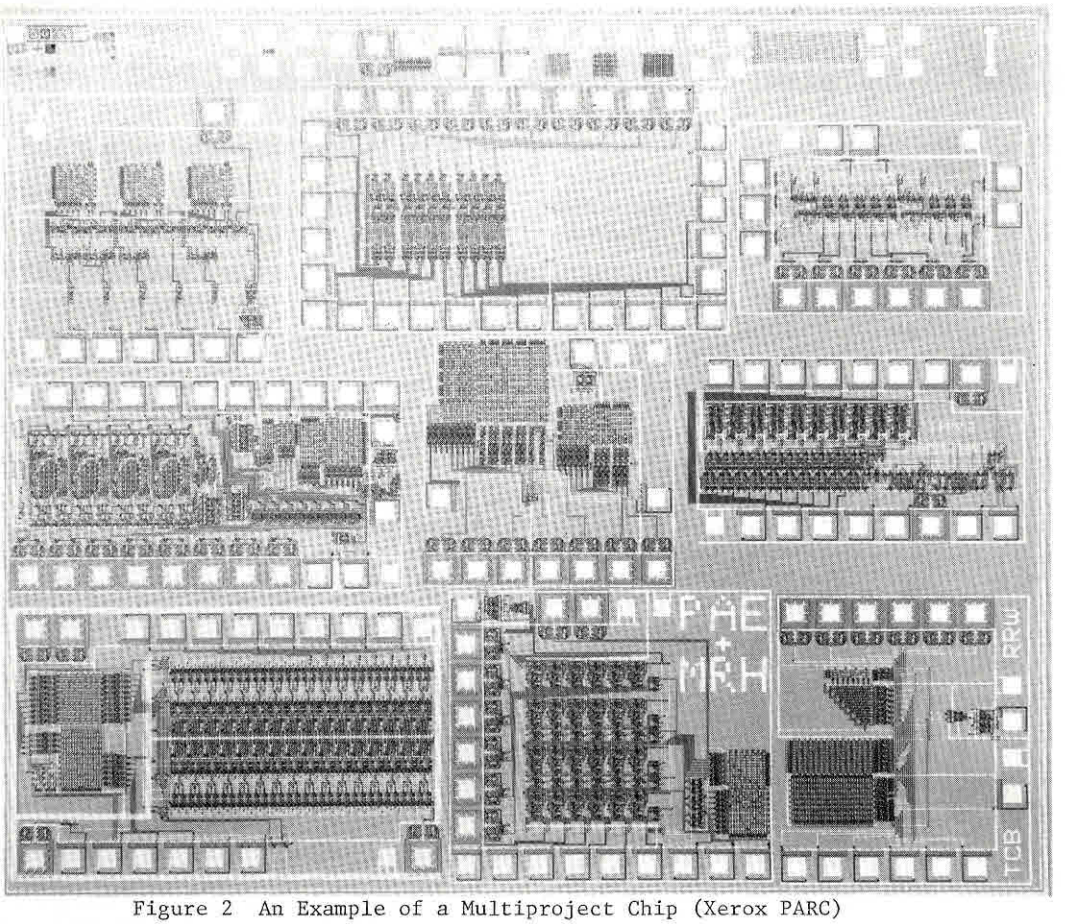

Figure 2 An Example of a Multiproject Chip (Xerox PARC)

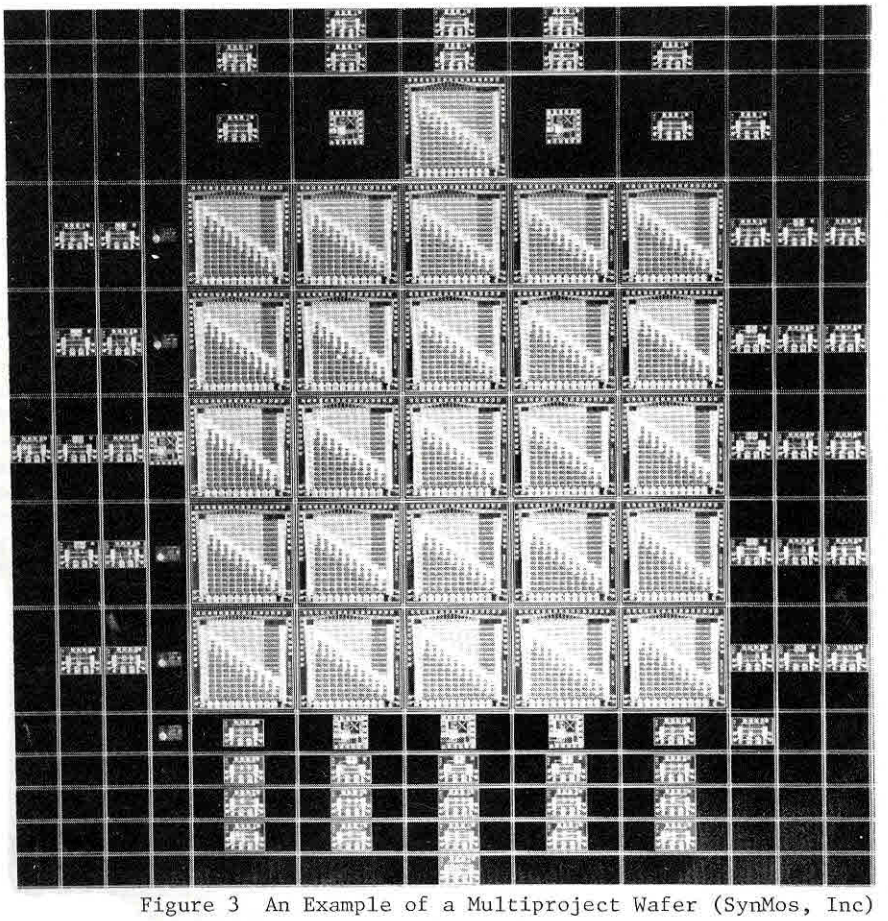

Figure 3 An Example of a Multiproject Wafer (SynMos, Inc)