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Design for VLSI — An Undergraduate Teaching Program

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SUMMARY Carver Mead and Lynn Conway in "Introduction to VLSI Systems" proposed a methodology which has simplified integrated system design to a point where some background in basic digital techniques and computing science is sufficient to enable a person uninitiated in integrated circuit design to proceed with and produce designs and layouts of moderate complexity. The above pioneering work not only has opened an entirely new research area in VLSI but also has provided for new challenges in the undergraduate teaching program that one may consider. This paper outlines the structure of a course developed for final year electrical engineering students and highlights some of the successes and pitfalls of such a venture.

1.0 INTRODUCTION

The recent advances in Very Large Scale Integration (VLSI) technology has opened up numerous research possibilities in realization of complex systems on a single chip. The rapid changes in both the size and complexity of integrated circuits have made it necessary to review many aspects of integration techniques from conception through geometric layout and fabrication.

The VLSI era that we have just entered is characterized by numerous problems that are related to both the devices and systems that utilize them. Thus new challenges appear on the horizon.

The pioneering work by Mead and Conway [1] and in particular, their approach to structured design has been a milestone in the evolution of VLSI technology. Their work has simplified the integration of large systems to a point where a reasonable background in basic digital electronics and computer science is sufficient to enable a person uninitiated in integrated circuit design to produce complex structures in a form suitable for integration.

The initiative taken by CSIRO's VLSI program in making available this newly acquired technology, to many research organizations and tertiary institutions has sparked a new awareness of the microelectronics evolution.

The collaboration between the Department of Electrical Engineering and the CSIRO's VLSI program has been a major factor in introduction into the Electrical Engineering syllabus an experimental course on VLSI based on M & C [1] approach.

This paper outlines the structure of this course which has been primarily for final year Electrical Engineering students, a portion of which was first introduced in 1981.

2.0 COURSE OVERVIEW

The course is structured as a three term unit based on Mead and Conway design approach to VLSI Systems [1]. It deals with the fundamental issues governing the design of VLSI components from problem definition, basic cell characterization, through to geometric layout and generation of magnetic tape in suitable format for mask making and eventual fabrication. [2]

The material during the first few lectures are related to derivation of a simple model for nMOS transistor. These results are subsequently used to estimate system performance in terms of propagation delays and power dissipation. Patterning and fabrication technologies are also studied at sufficient depth to ensure adequate understanding of the underlying principles on which nMOS design rules are based upon.

Particular emphasis is placed on the importance of regular structures which are configured using small numbers of basic logic cells. The problem associated with communications paths are also highlighted by working through several simple examples such as barrel shifter, parity generator, bus arbitration logic and so on. Attempts are made to illustrate that communication costs are high in silicon and therefore an understanding of the above fundamental issues which govern the design and layout, need to be considered from the beginning.

Other topics such as data management, distribution of function and interface to the designer are also examined.

2.1 "Hands on" Approach

An increasing proportion of the teaching in the electrical engineering/computer science area is becoming dependant on "hands on" aspects for effectiveness. This is particularly true in, say, the microprocessor area where the fundamental aspects of digital processors, computer architecture and so on are really only learned by working experience with microprocessor based equipment. Furthermore, if teaching is to proceed beyond an elementary level then success or otherwise is generally dependent on reasonable back-up facilities in the form of hardware, software and computer systems.

The same factors apply to the teaching of design technique for VLSI. The lectures are supported by a series of "hands on" excercise/project work in which the student must work through well chosen problems which provides both a feel for the underlying technology and for the design methodology. It is also a distinct advantage to have some simple software aids and computer systems at this introductory level at which design is proceeding at the mask

level. It is found distinctly beneficial if participants work in small groups of 2 or 3. Further, it is essential to have an adequate number of demonstrators available to deal with questions as they arise on a group basis. One demonstrator per five groups is possibly the figure to aim at in this respect.

Currently plans are on the way for the students to participate in Australia's first multi-project chip AUSMPC82 [3]. The projects include, reorderable memory architecture, adaptive filter, and various type of signal processing structures. The designs are modular which permit several students to work concurrently on the same project.

3.0 DESIGN STATIONS

Two approaches have been implemented in the setting up of design stations to satisfy the needs for implementation of student projects of moderate complexity. The first method utilizes the interactive colour graphics system which has been developed by several postgraduate students during the last few years [4] - [6]. The system as shown in Figure 1 consists of a NOVA computer, Universal Layout System (ULOS), and a data tablet with a stylus. The ULOS is an interactive graphics display processor which is tied to NOVA as a peripheral device. Its function is to output video signals to the graphics terminal. A resolution of 512 × 512 with eight different colours is achieved in this configuration.

In terms of software, the control of NOVA and ULOS is given to the I.C. layout program MDESIGN [7]. Once MDESIGN is evoked interactive design phase via the stylus on the data tablet commences. The user views his designs on a colour display and is able to implement modifications through the data tablet.

Once a design is completed, the picture file is transmitted to the University's Cyber computer. At this stage the data can be converted into Caltech Intermediate Form (CIF) by a locally written program ITOC [9]. The CIF file, if required, may subsequently be loaded onto a magnetic tape ready for the next phase.

Although interactive colour graphics terminals allow rapid realization of systems, their cost prohibits their use in organized tutorial sessions.

In addition the throughput of this system is low since the students are required to work serially. Therefore in order to overcome such limitations, a second approach which utilizes the University's VAX computer in conjunction with a H.P. multi-pen plotter has been implemented. The students are given access to a low level symbolic layout program BELLE [10]. The function of BELLE can be likened to that of a macroassembler in which the user defines symbols (i.e. macros) to describe the layout.

On completion of the layout, the design is contained in system layout files in Intermediate Form. In order to facilitate checking of the layout, a checkplot of the layout is generated by converting the design files onto files for driving the H.P. plotter.

This arrangement enables up to fourteen users to work concurrently.

4.0 SOME ASPECTS OF FUTURE COURSES

One of the aspects of "hands on" process of learning which is more difficult to achieve is that of direct feedback on the success of design work either by having designs evaluated and criticised by others more expert in the field or by having designs fabricated and the I.C. chips fedback to the students for their evaluation of performance. This latter possibility can be implemented through concepts such as the multi-project chips (MPC).

For more advanced courses where architecture rather than IC mask level design is required, it is advantageous to have available more sohpisticated design aids for teaching. These could include several interactive colour graphics and or interactive monochrome graphics design stations with suitable support software and a library of properly characterized and tested "standard cells". The standard cell concept is most important otherwise a disproportionate amount of time is wasted in mask level design. One finds that simulation is also essential at this level.

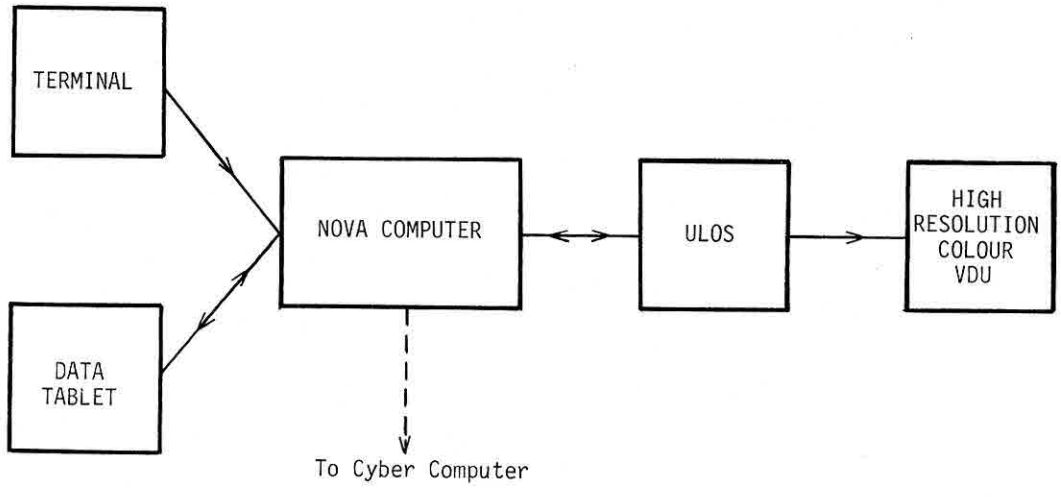

Figure 1 Colour graphics design station

Finally, all courses should be configured and constructed in such a way as to accommodate different aspects of technology, for example, courses should not be restricted to nMOS alone but rather should be readily adaptable to say CMOS or I^2L designs or other technologies as the need arises.

5.0 CONCLUSIONS

Although the current VLSI teaching program is still in its infancy, interesting challenges appear on the horizon. The enthusiasm shown by students who so far have participated in this experiment has been very encouraging and perhaps points to the success of the course. However the final assessment still rests with the results of the Multi-Project Chip [3] to be evaluated sometime in September 1982.

6.0 REFERENCES

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