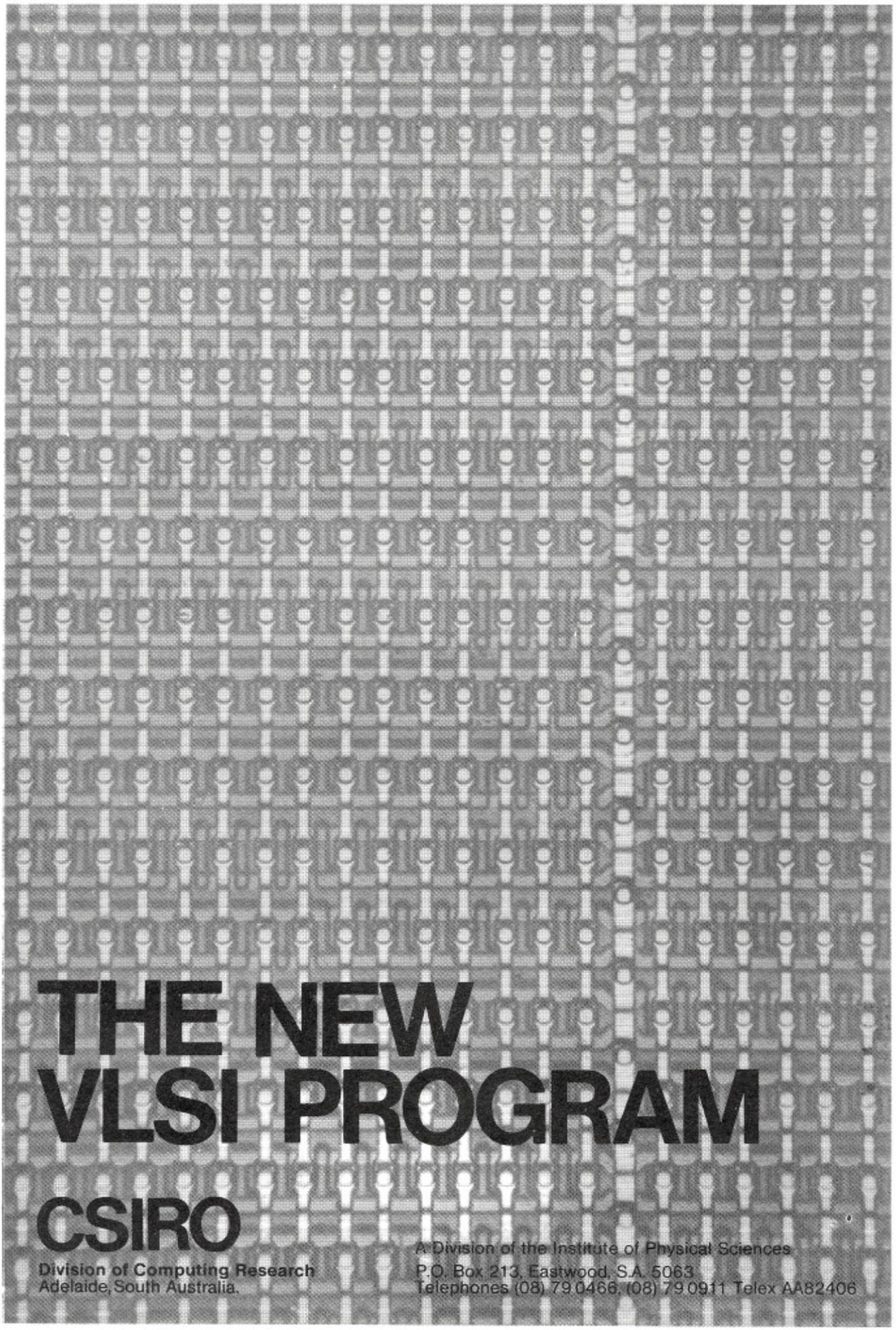
THE NEW
VLSI PROGRAM
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CSIRO'S NEW VLSI PROGRAM

In 1981, the Australian federal government's research arm, the Commonwealth Scientific and Industrial Research Organisation (CSIRO), established a new unit in its Division of Computing Research. Known as the VLSI Program, it is a microelectronics research effort in the design of VLSI (Very Large Scale Integrated) circuits. Such circuits have of the order of 100,000 transistors per chip. Initial funding for the program is $1.5 million.

The goals of the VLSI Program are:

1. to establish a design centre with an international reputation in VLSI design,
2. to demonstrate this capability by the design and remote fabrication of a 100,000 transistor chip, and
3. to facilitate the development of a design technology for Australian industry,

within three years.

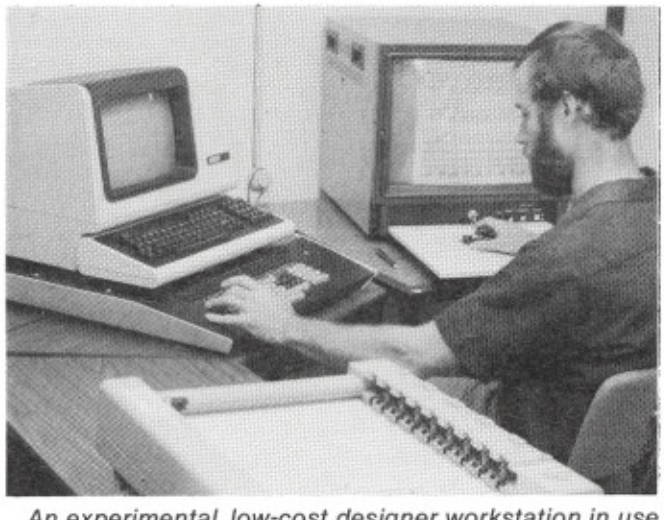
Research is being done in the following areas: composition systems, hierarchical verification, symbolic layout, chip assembly, concurrent chip architectures and distributed computer-aided design (CAD).

The group will focus on the complexities of chip design, and will not establish facilities for the manufacture of chips. Experimental designs produced by the group will be implemented by mask-making and wafer-fabrication facilities in Australia and overseas.

The 100,000-transistor chip, to be designed in 1983 to demonstrate the group's design capability, will also act as a vehicle for research in design measures and concurrent architecture. Several candidates for this vehicle are being considered in 1982.

The technical bases for the group are recent breakthroughs in structured chip design in the United States. The CSIRO initiative is led by Dr J. Craig Mudge, an Australian. He played both technical and managerial roles (at California Institute of Technology and the VLSI Advanced Development Group at Digital Equipment Corporation) in some of these breakthroughs in the U.S.

At full strength, the group will have 15 members (plus overseas visitors) with expertise split equally between the disciplines of computer science and electrical engineering.



An experimental, low-cost designer workstation in use at CSIRO. Components include a colour-graphics display, alpha-numeric display, keyboard, pointing device, and a colour plotter. This workstation, linked to the lab's VAX-11/780, is the designer's primary interface to his computer-aided design environment.

EQUIPMENT

The VLSI Program is being equipped to the same level as other international laboratories in the chip design field. A two-megabyte VAX-11/780 (with 512Mbytes of disk storage) is the laboratory's chip-data-base machine and component of a local distributed CAD system. Communication links to a variety of CSIRONET hosts (Cyber 76, for example) form the basis of an electronic-mail link with Australian collaborators and a possible national distributed CAD system.

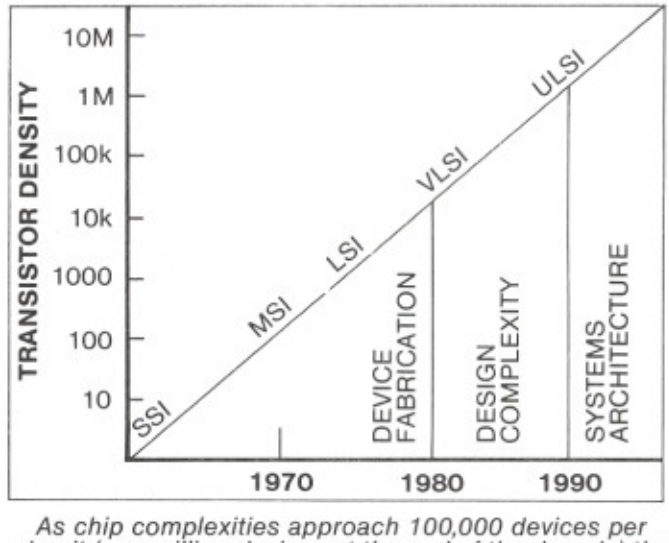
Other equipment includes two colour-graphics designer work stations, several plotters, a digital electronics laboratory for prototyping, analysing, and testing chips, and electronic-mail and word-processing terminals.

SCIENTIFIC EXCHANGE

Research collaboration in design methodology is underway with several universities in the U.S. including UC Berkeley, California Institute of Technology, and Stanford University. Important research links with VLSI Technology Inc., a new silicon foundry in California, and XEROX Palo Alto Research Centre have also been established.

In Australia, the new group is working with other divisions of CSIRO (Radiophysics and Manufacturing Technology, for example), Australian industry, tertiary educational institutions, and government research laboratories.

Several members of CSIRO's VLSI Program have taken part in the organization of the technical programme of Microelectronics '82, held in Adelaide in May, 1982. The conference, sponsored by the Institution of Engineers, Australia, is the country's first national conference on future silicon chip technology. Topics covered include processing technology, computer-aided design, testability, packaging, and concurrent architecture. Over fifteen speakers are from overseas.



As chip complexities approach 100,000 devices per circuit (one million devices at the end of the decade) the limiting problem has shifted from fabrication to design time. Unless rapidly escalating design costs can be contained, the full potential of silicon technology will not be realised.

COMPLEXITY MANAGEMENT

The steady increase of transistor density, which has brought us to the beginning of the VLSI generation of technology, shows no signs of slowing. By the end of the decade we expect to be designing single-chip structures containing one million transistors.

However, escalating design costs are restraining full application of this technology. In the LSI era, design costs of 50 man-years per chip were common. If the design methodologies used then are not improved, we face costs of 1000 man-years in the mid-to-late 1980's. Such costs are prohibitive for all except those designs sold in ultra-high volume. Much of the VLSI Program's research is directed at reducing design time (to a few man-years for VLSI chips, to a few man-months for simpler chips).

VLSI is a statement about system complexity, not about transistor size or circuit performance. VLSI defines a technology capable of creating systems so complicated that coping with the raw complexity overwhelms all other difficulties.

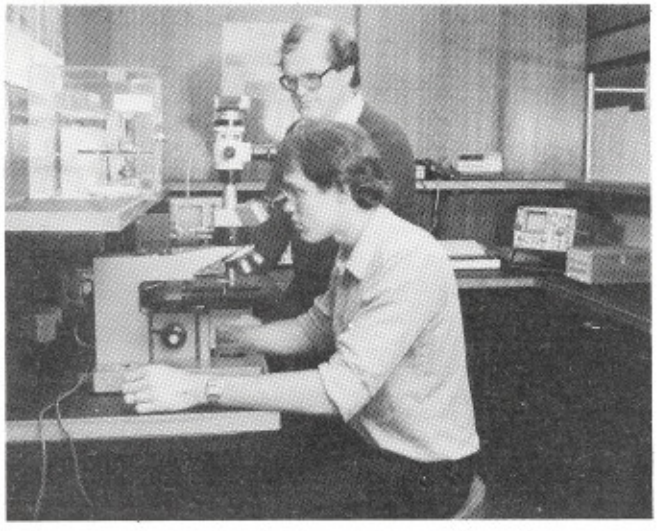
Several different design representations exist for a large chip, some schematic, some textual, and some visual. Most important are mask artwork (layout), circuit, logic, and floorplan. A VLSI chip data base will contain between 5 and 15 million bytes of information (counting each representation of a design).

New design methodologies, computer-aided-design (CAD) tools, and design representations are being explored. We have been influenced strongly by the pioneering work of Professor Carver Mead (California Institute of Technology) and Professor Lynn Conway (XEROX Palo Alto Research Centre and Massachusetts Institute of Technology).

We model a complex circuit by viewing it as a tree structure of rectangular leaf cells (typically 20 to 100 transistors each) and composition rules. Methodologies and tools for composition are the thrust of our research and system building in computer-aided design. Our tools for leaf-cell construction and analysis were evaluated on a small (2000 transistor) design late in 1981. They include a procedural layout language, a geometric editor, and tools for design-rule checking, circuit extraction, circuit simulation, switch-level simulation, and logic simulation.

Constrained layout rules, e.g., shapes formed from 90 degree angles only, allow more tractable CAD programs, and are gaining in popularity. The sheer size of a chip database and the number of independent programs (around 20) in a CAD suite mean that attention is being paid to bookkeeping programs for designers.

Silicon compilers (a few prototypes exist overseas) are a promising longer-term solution to the design problem.



Research staff using the VLSI Program's analysis laboratory.

MULTI-PROJECT CHIP

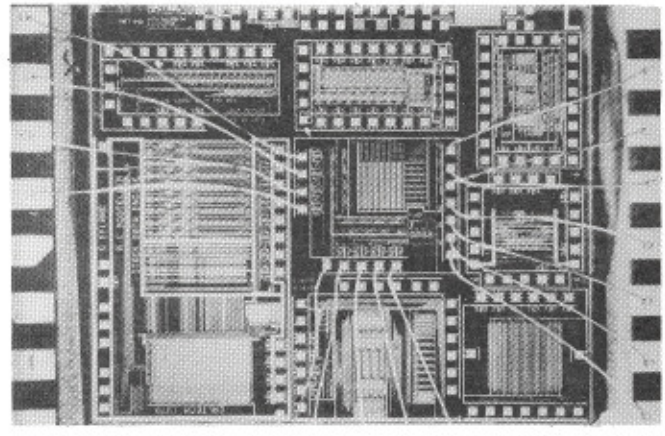
Following the introduction of Mead and Conway integrated-circuit design courses into Australian teaching institutions, a rapid increase in design activity has occurred. To complement this, CSIRO has designed a chip implementation system for the rapid, remote fabrication of experimental designs.

By combining the pattern-generation files of many independent designs to form one mask set, fabrication costs are reduced by an order of magnitude. While a fabrication run for a single design might cost $40,000, a shared run can be done for around $50,000. The components of the implementation system are
(a) a standard interface to fabrication; and
(b) information and logistics management. The first fabrication run will use electron-beam masks, a five-micron nMOS process, and a forty-pin package.

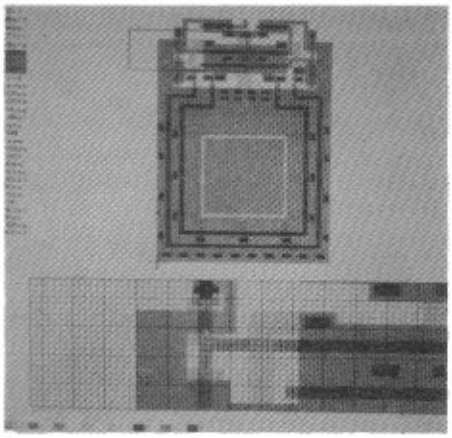
May 31, 1982 is the cut-off date for designs to be implemented on Australia's first multi-project chip (AUSMPC). Twenty-five institutions (4 industry; 16 education; 5 government research) are involved.

Although there is space for 40 average-sized designs (around 2000 transistors each), this first attempt has been significantly over-subscribed. Designs submitted include:

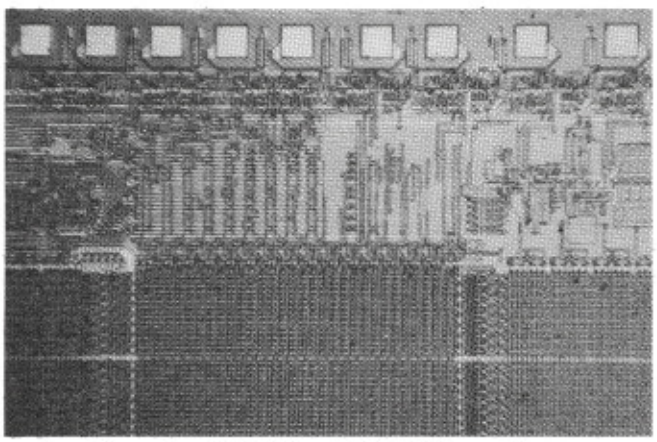
- signal processor for radio-telescope data
- computer graphics clipper
- hearing prosthesis prototype
- switch block for telecommunications
- (several) digital filters
- borehole logging probe
- highly parallel adder
- eye movement detector
- image analyser
- computer disc controller
- local network arbitrator
- vision processor sub-section
- electro-cardiogram pattern recogniser



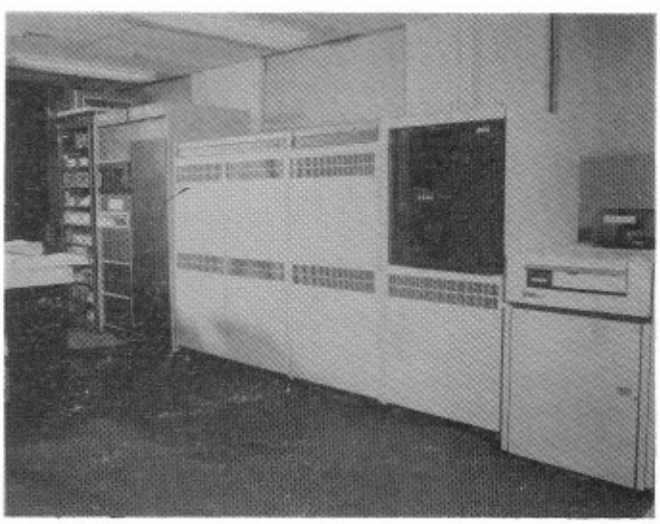
A Multi-Project Chip (MPC): eight independent designs sharing a fabrication run. The centre design has been bonded (input-output connections wired). Other copies of the same chip would be bonded for the other designs. The row of test structures along the top of the chip is a key part of the standard interface to fabrication. [This chip is from the first U.S. multi-university multi-project chip (MPC79)].



The designer uses a graphics editor to design bottom level cell geometry. In the screen centre is the layout for a connection pad, below it a magnified section, and to the left a menu of editor commands.



A portion of an LSI chip of 10,000 transistors.



This VAX-11/780 is the chip-data-base machine for the VLSI Program in Adelaide. Computers are used extensively to aid the design process; a typical VLSI chip data base contains 5 to 15 million bytes of data. The Adelaide CSIRONET node, enabling an electronic-mail link to Australian collaborators can be seen on the left.

CIRCUIT/PROCESS TECHNOLOGY

Two distinct processes are in use by the VLSI Program: a robust MPC process and a research process for the 100,000-transistor demonstration chip.

A five-micron n-channel MOS silicon-gate depletion-mode-load technology is the 1982 MPC process. In 1983, both CMOS and nMOS (at 4-micron channel lengths) will be available for AUSMPC designs. For each of these processes, the design rules are standard, lambda-based, Mead and Conway rules.

The research process (for 1983-84 fabrication) is a two-micron NMOS process with two layers of metal. Sufficient characterisation of this process exists for us to predict performance at the overall chip level; more detailed characterisation will be completed by early 1983.

POTENTIAL APPLICATIONS OF VLSI

Because of its applications, engineering skills (in both electronics and computing), Australia has an opportunity to exploit user-designed silicon. Areas which appear well matched to the new technology include medical electronics, signal processing for oil and mineral exploration, animal-borne instrumentation, radio-telescope signal processing, telecommunications, and computer vision.

Because of the tremendous expense (to date) of designing complex integrated circuits, traditional semiconductor manufacturers prefer to develop only products that can be sold in large volumes, memories and standard microprocessors being the best examples. With the advent of new design techniques and the availability of shared fabrication runs, low-volume chips become economically feasible.

ADELAIDE, SOUTH AUSTRALIA

CSIRO's VLSI Program is located in Adelaide, the capital of South Australia, one of the least populated states (about 8% of Australia's 14 million people). Adelaide, a gracious and cultured city, is an ideal place for high-technology researchers to work and live. Its performing arts complex, the Festival Theatre, is acclaimed as being one of the best in the world. The outdoor life is close at hand, with many beaches, and bushland in the Adelaide Hills and not-too-distant Flinders Ranges. Adelaide is a capital city free of the overcrowding of Sydney and Melbourne. Its nearby wine-growing areas produce two-thirds of Australia's wine.

In the formative stages is Technology Park Adelaide. It aims to enhance South Australia's established base in mineral research, microelectronics, defence research, manufacturing technology, medical and agricultural research.

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