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A MILESTONE FOR CSIRO IN TECHNOLOGY TRANSFER IN SILICON CHIPS

CSIRO has just completed a major step in technology transfer in one of the fastest developing technologies of the 1980s - the design of silicon chips.

First-time chip designers from all over Australia have just received their chips from CSIRO. The designers, practising engineers in Australian industry and research laboratories, and students in universities and institutes of technology, learned the new design technique following an intensive 3 week course for lecturers in Adelaide in February.

The overseas fabrication of forty-six Australian designs has been accomplished by Australia's first Multi-Project Chip implementation system, designed and coordinated by Robert Clarke of CSIRO's new VLSI Program.

Innovative new applications of microchips in medical electronics, minerals exploration, telecommunications, and computer control have been discovered by this Australian design activity. Forty-six designs from 21 participating institutions were fabricated.

CSIRO's role was twofold: teaching and coordinating the multi-project chip fabrication system. Lecturers attending the February course are now teaching courses for both students and designers from industry.

In 1981, CSIRO established the VLSI Program in Adelaide, in its Division of Computing Research. The new group was formed to conduct research in the design of Very Large Scale Integrated (VLSI) circuits. In the VLSI era of microelectronics, it will be possible to fabricate chips containing 100,000 transistors on a single 10mm square of silicon. CSIRO's research at the leading edge of technology has an added benefit: spinoff to the design of less advanced, ie less dense, chips *(as* shown by the MPC designs). Most of these smaller designs have densities of around 2000 transistors each.

The chip design technique introduced into Australia by CSIRO is based on the pioneering work of Professors Carver Mead and Lynn Conway in the United States.

According to Dr J Craig Mudge, the head of CSIRO's VLSI Program, "prior to this demonstration in Australia, the conventional thinking was that chip design was the province of a handful of experts within the traditional chip-manufacturing firms. The mystery of chip design has now been dispelled. We have shown that researchers and engineers, expert in their ·clum application fields, can learn to design and apply silicon in a matter of months".

Dr Mudge, an Australian computer scientist, spent 12 years in the United States designing computers and, later, pioneering VLSI design research.

The MPC implementation system available to Australian designers has two motivations: costsharing and a standardised interface to manufacturing. By combining the pattern-generation files of many independent designs to form one mask set, fabrication costs are reduced by an order of magnitude. While a fabrication run for a single design might cost $40,000, a shared run can be done for about $50,000 (representing $2000 each for 25 designs).

This first MPC has shown that it is possible for an Australian researcher or engineer (an expert in his own field, but not a chip-design specialist) to design a specific chip for his own application.

The steps in an MPC implementation system are checking, merging, maskmaking, wafer manufacture, packaging, and test measurement. Some steps were done in Australia, some in the US. The information management steps were carried out by CSIRO. An Australian firm, Philips, performed the packaging step (breaking the wafers into their constituent chips, mounting the chips in ceramic packages, and connecting hair-width gold wires from the silicon to the external package connections). Electron-beam masks were made in California, and wafer fabrication (requiring equipment worth' $50m) was also done in the US.

An electronic-mail link, using CSIRONET, was established to allow communication between the VLSI Program and the design community.

A whole new field is now open to Australian industry (for application in its products and processes). In addition to using standard chips, engineers can now design their own custom chips. About 60% of the designs on this first MPC implement functions not possible with standard chips.

The first MPC closed on May 30, 1982 (ie designs had to be in Adelaide by that date). Chips were returned in mid-August, according to the promised schedule of two-and-a-half months. A second MPC will close on November 30, 1982. By the end of 1983, CSIRO hopes to be running four MPC implementations per year.

J. Craig Mudge .
12 August 1982

The 46 designs on Australia's first Multi-Project Chip system
May 31. 1982

CLASSIFICATION BY APPLICATION

Project No	
	MEDICAL
13	Cochlear implant receiver/stimulator
43	ECG pattern recogniser
58	Controller for an insulin diffuser
59	Highly parallel cell image analyser
15	video analyser for eye-movement detection
	COMPUTER GRAPHICS
11	Comparator for clipper
77	Graphics layout controller
	COMMUNICATIONS
12	Subsystem blocks
56	PCM signal and line code generator
78	Time-division switch
79	Error rate monitor
66	Serial data matrix transposer
72	Bus arbitrator
	CIRCUIT/PROCESS TEST STRUCTURES
	RAM
2	4-bit datapath
5	Function block
6	Poly/metal runs
8	Analog test structures
9	Analog sensors
10	D/A converter
33	Monostables
34	Analog output stage

SIGNAL PROCESSING
24 Low pass recursive filter
14 Generalised adaptive filter
17 Signature analyser
74 second-order digital filter
60 Smart sensor array

ROBOTICS
52 Connectivity analyser for vision

MINERAL EXPLORATION
54 Controller for borehole multi-channel analyser

RADIOASTRONOMY
67 Integrated linear interpolator
80 Autocorrelator

COMPUTER ARITHMETIC
3 Serial multiplier
4 Transcendental function generator
7 Pipelined multiplier
45 Adder tree (time)
75 Adder treee (space)
49 Mersenne transform
53 Pipelined multiplier
69 Sine/cosine generator
71 Decimal adder
25 1-bit adder latch

COMPUTER BUILDING BLOCKS
30 Self-timed data sorter
20 Four-bit datapath
61 Two-dimensional shift register
85 Memory management unit
116 Registerfile for seial microcomputer

II CLASSIFICATION BY TYPE OF INSTITUTION

The 46 designs came from 20 institutions (5 designs from industry). The breakdown on institutions is as follows:

Industry	3	
CSIRO divisions	3	
Universities	11)	Research Designs
Institutes of	)	and
Technology	2)	Student projects
Government labora-	1	
tories		
	20	

III ATTRITION AND SELECTION

There were 85 bids for space; 82 were still alive May 3. 60 designs were submitted May 30, 46 obtained space.

J Craig Mudge 3
June 1982