The Results of AUSMPC 5/82

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Between July 1981 and September 1982, Australia moved from a position of having no user-designed custom integrated circuit capability to the point where forty-six designs from twenty-one institutions were conceived, executed, fabricated, and tested. Over a hundred designers (from tertiary educational institutions, industry, government laboratories, and other CSIRO divisions) were trained, and several design centers were established. Thanks to AUSMPC (Australian Multi-Project Chip) 5/82, several innovative applications for custom circuits were discovered in medicine, minerals research, and communications, most of them by first-time chip designers.

The Implementation System

Figure 1 shows a flowchart of the implementation. Because AUSMPC 5/82 was the first multi-project chip effort in Australia, we provided a back-up for each step. Hence, two sets of masks were made, two wafer-processing firms were used, and wafers were packaged both in Australia and in the U.S.

Because the design methodology we were introducing into Australia was new, few institutions had the necessary design tools. It was therefore decided to provided a basic set of tools to all participants in AUSMPC. Three design tools were written and distributed: the procedural layout language BELLE (Clarke 1982), a programmable logic array generator, and the plotting program VIEWCIF. (BELLE is a Pascal-based embedded geometric design language, based on Caltech's LAP.) To concentrate the effort on systems design, and to minimize duplication of effort, a library containing many important subcircuits was also distributed.

Centralized Design Support

Centralized design checking was offered to all participants in AUSMPC 5/82 during the three weeks before design cut-off.

All partial or complete designs submitted to CSIRO during this period were run through geometric design-rule checking, circuit extraction, and electrical-rule checking software, operating on the VLSI Program's DEC VAX 11/780 system. If an input file was supplied, the design was also run through a switch-level simulator.

Forty-five of the forty-six designs passed geometric design-rule checking in the active circuit area. One design, using geometries on half-lambda grid points, confused most of the design tools. Imaginative logos injected many (non-fatal) design-rule violations.

Circuits were simulated and electrical rules were checked for 75% of the designs submitted. These procedures served as an introduction to design analysis for many first-time participants.

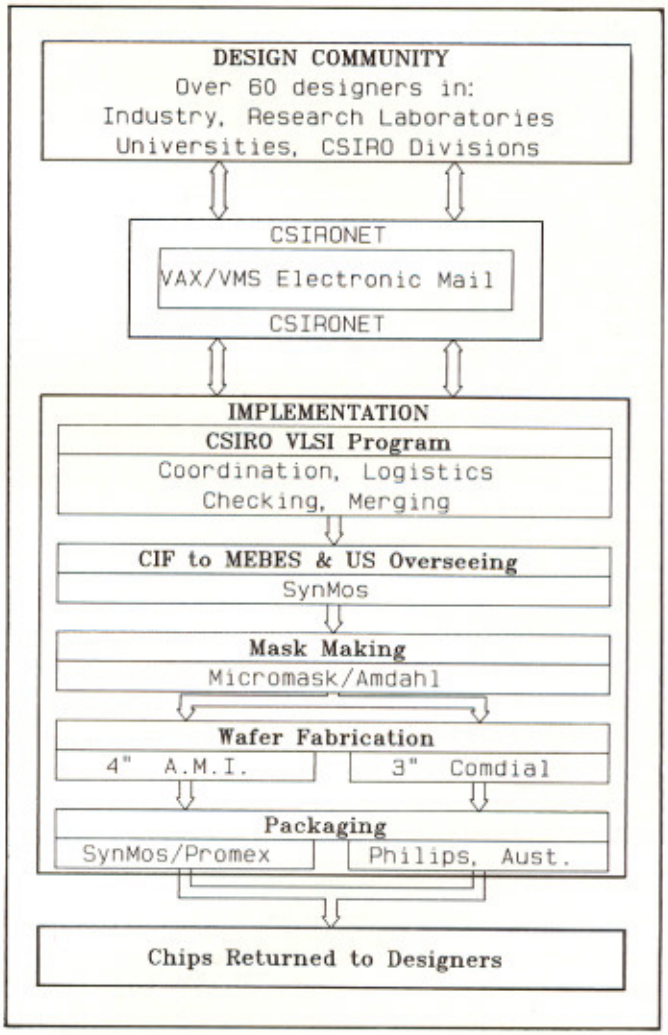

FIGURE 1. A flowchart of the AUSMPC implementation.

After elementary connectivity errors were eliminated, useful results were obtained. Some diagnostics from the electrical-rules checker (used by 24 designers) required interpretation in the design context to establish whether a real design error had been detected.

Five Design Classes

By identifying levels of abstraction for circuit behavior, we classified the designs by method. The 21 designs in Class A were mainly student designs; the 10 Class B designs adhered to pure Mead-Conway methodology, relying on the tau model (Mead

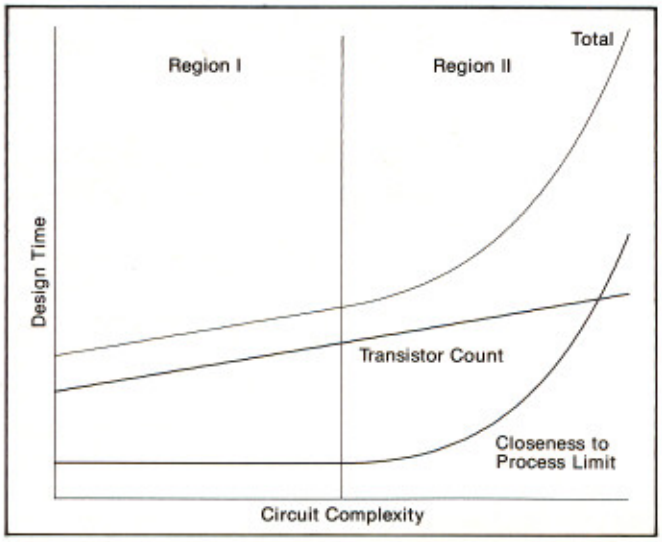

FIGURE 2. When chip area and speed are close to the process limit, design time increases exponentially.

and Conway, 1980); in the 8 Class C designs, the basic Mead-Conway approach was extended to include circuit simulation. Designs such as the static RAM, pipeline multiplier, and transcendental function-generator were in this class. A separate class, Class D (5 designs), was created for analog designs because of the difficulty of designing such circuits to meet standard fabrication procedures. The final class, Class E (2 designs), contained test structures to explore systematically the variations in wafer-process parameters.

The average design time for circuits in classes A and B was 260 man-hours, whereas Class-C designs averaged 330 man-hours. There appear to be two major determinants of chip-design time: the transistor count (raw complexity), and the closeness of performance (area and speed) of a particular process. The use of a structured design approach can keep the design time linear with transistor count. However, an exponential increase in design time occurs when a design approaches process limits. Figure 2 shows how these two factors affect design time, and distinguishes two regions of the design space. AUSMPC designs in classes A and B were operating in Region I, whereas most of the designs in Class C fell into Region II.

Testing Results

Forty-three of the forty-six designers submitted testing reports; of these, twenty-five reported 100% success. Figure 3 shows the success rate by design class. The value of functionality was obtained by dividing the number of working functions in a design by the total number of functions in that design. (Speed was ignored in this measurement, but is discussed below.) The most common errors were logic errors and the shorting of power and ground.

Two simulation programs were available to designers: the circuit simulator SPICE (Nagel 1975, and Vladimirescu and Liu 1980) and a switch-level simulator similar to Bryant's (1980). Thus, Figure 4 shows four groupings by type of simulation. The fourth group (switch-level simulation only) had a higher success rate than the third group, which used both simulators. An explanation for this difference may be that the third group contained more difficult designs.

Unfortunately, there was no historical data upon which to

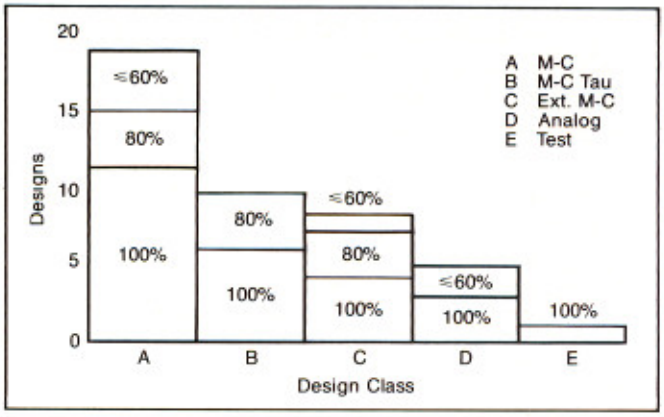

FIGURE 3. Success rate by design class (percent functional).

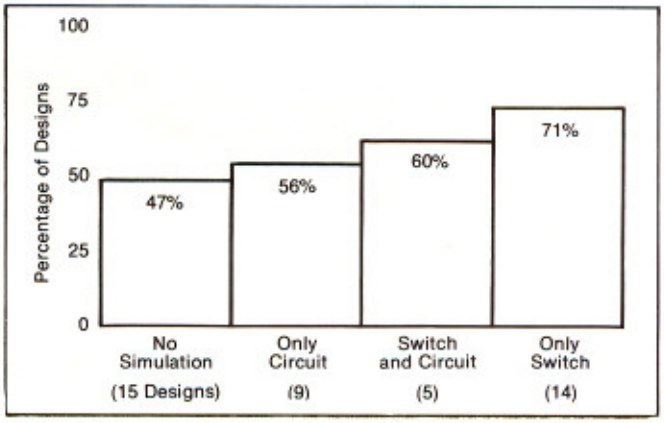

FIGURE 4. Success rate by type of simulation (percentage of completely functional designs).

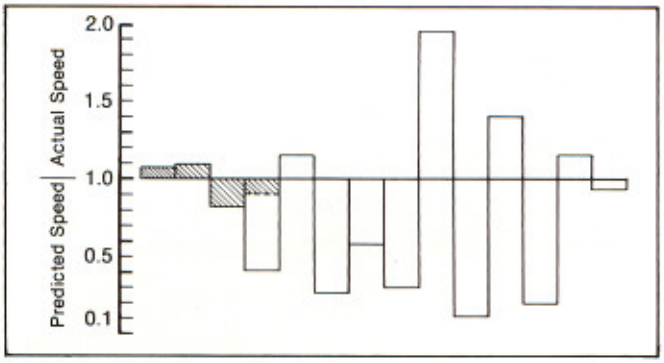

FIGURE 5. Ratio of actual speed to predicted speed for fourteen designs. Cross-hatching indicates comparisons to SPICE predictions.

base our transistor models. Therefore, we created our own models (see box: Transistor Models for AUSMPC 5/82).

Only fourteen of the designers documented their speed predictions when submitting their designs at the end of May. Figure 5 shows the ratio of actual speed of operation to simulated speed; thus, for example, the second design ran 10% faster than predicted, and the eighth design ran only 30% as fast as predicted. Measured speed is the average of chips from the two wafer-processing sources. (The differences in speed between the two sources were surprisingly small—less than 33%.) The cross-hatched areas in Figure 5 indicate the four designs that used SPICE; the narrow spread is encouraging. Two values are shown for the fourth design, because the designer originally

A Sampling of Chip Designs

Hearing Prosthesis Receiver/ Stimulator Prototype ("Bionic Ear")

Hugh McDermott, Dept. of Otolaryngology, Univ. of Melbourne

This chip is an nMOS prototype of the implanted component of a hearing prosthesis receiver/stimulator for the profoundly deaf. The implant is located behind the ear, and stimulates the auditory nerve through an array of 20 electrodes inserted into the cochlea. Digital control signals (57 bits per message) and electrical power are transferred from an external speech processor through a transcutaneous inductive link. This prototype design will be later redesigned in CMOS, a more suitable technology for human implants.

Multi-Channel Analyzer Controller

Ian Smith, Australian Mineral Development Labs, Adelaide

The AUSMPC design is an integrated controller for spectral-acquisition processing in a bore-hole logging probe developed for mineral identification at depths exceeding 1 kilometer. Identification involves spectral analysis of the radiation back-scattered by material in the bore-hole walls next to an on-board neutron source. Outputs from scintillation detectors in the probe are processed to determine the energy level of received particles, and a corresponding memory location is then incremented to build up a spectral-energy distribution curve.

Modular Cross-Correlator

John Ables and Andrew Hunt, CSIRO Div. of Radiophysics, Sydney

This project is a prototype implementation of a fully parameterized design for a modular cross-correlation processor. The design is expressed in BELLE. The size and function of the correlator design are controlled by only three program variables.

The chip will be used first for direct, single-dish, aperture-synthesis signal-processing for radio-astronomy. In 1988, expanded versions of the design will be used in the national Australia Telescope. The prototype is a 2x2 implementation. An 8x8 version, handling 64 channels, was submitted in the November AUSMPC. Correlation systems implemented with this chip demonstrate the power of circuit integration: a 1024-channel TTL version for the Australian National Radio Astronomy Observatory required approximately 2kW of power. It can be replaced by a system containing just 16 of the 8x8 versions of the chip.

An Image Sensor for Hadamard Transforms

Trevor Cole and Colin Jacka, Electrical Engr., Univ. of Sydney

This design combined photo-detection and processing to let the Fast Hadamard Transform of linear images be obtained directly from a chip exposed to an optical image. The effects of light on nMOS charge-storage nodes can be used in photo-detection applications, as Lyon (1982) did with the optical mouse.

The Hadamard transform is especially useful in reducing the effects of transmission-channel burst noise on picture quality, by distributing the transmission times of adjacent pixels over the picture-transmission interval. The chip can also be applied to image-transmission bandwidth-reduction schemes, by selectively transmitting significant features.

A Fast nMOS Static RAM

Marcus Paltridge, CSIRO, VLSI Program

This design explores circuit techniques in memory design. It studies bootstrapping techniques intended to drive pass-transistor logic above V_{dd} and hence increase circuit speed; differential signaling techniques for rapid detection of signal changes, and driven enhancement/depletion techniques for fast on-and-off chip drivers to make interfacing easier.

ignored the capacitance value of a long polysilicon run. After circuit testing, he revised his circuit simulation, and obtained the much closer simulated value shown.

Analog Circuits

To date, there is no satisfactory standard interface to fabrication for analog circuits, because the electrical behavior of such circuits depends critically upon process knowledge. Therefore, we were pleased with the success of McDermott's cochlea implant design, which depended on a high proportion of analog circuitry. Because many VLSI circuits interface both analog and digital processing (particularly in the communications and medical fields), there is clearly a demand for an MPC implementation service for analog design. To this end, Malcolm Haskard, on leave from the Microelectronics Centre of the South Australian Institute of Technology, devised a set of test structures (13.3 sq mm in total) to study the major analog functions (amplifiers, comparators, filters, voltage and current references, and analog-digital converters). Based on his preliminary results (Haskard 1983), he recommends the following procedures for analog design in an MPC environment:

1. The use of self-biased inverting-type amplifiers, because conventional (differential) op amps have offset-voltage and dynamic-range problems.
2. Switched-capacitor techniques instead of resistor matching methods, because of the wide spread in resistor parameters, and because of the low sheet-resistance values.
3. A polysilicon-metal capacitor instead of a gate-implant capacitor, even though the former uses approximately eight times as much area. The gate-implant capacitor requires an extra mask step, and has poorer temperature and voltage coefficients than does a poly-metal capacitor.

The Next MPCs

A second AUSMPC closed November 30, 1982; regularly scheduled MPCs will be conducted in 1983. Some of the designs on the November MPC include an interpolator for scan conversion; several elements of a formant extractor for speech processing, a raster-display synchronizer; a photodiode array for acousto-optical signal processing; an address management unit for a complex number vector processor, and a serial floating-point adder. □

Acknowledgments

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