6.978 Lecture #7. Tuesday Oct 3

Today: Some more circuit & delay calculations which affect layout geometries ... sys. designs

(i.e., now that you know what layout is like, you see why its a good idea to have things in order at the higher levels before committing to all that work ! ! !)

Thurs: Subsystem, circuit, stick, & layout of several interesting subsystems.

(examples, on order of small to moderate project)

[NO CLASS NEXT TUESDAY]

How are designs are implemented (intro)

Thurs (next week): How to describe layouts: use of symbolic layout language.

- Hand in HW #3

- I'll handout HW #4 next time. I want to see how you did with those layout problems first --- probably will be a stick + layout of one for

- Start thinking about projects. During next few weeks you'll find all the tools you need to begin. Also we'll see many examples. Perhaps sketch out any ideas of interest. I urge you all to find collaborators: for at least designing. Talk to others - it may help you get in the - if you have more than one idea - slot with others. I will hand out a questionnaire sometime soon to see how you are coming on these preliminaries. Constraints, Alternatives, Past History?
Discuss HW #2 before we begin lecture:

As we'll see later, our old friend the "Selector circuit" will run up to have many uses when installed in different ways. A solution to 5(a) is to reverse the input/output, and hook up VDD & GND:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Z₀ (out)</th>
<th>Z₁</th>
<th>Z₂</th>
<th>Z₃</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>01</td>
<td>111</td>
<td>10</td>
<td>11</td>
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<td>111</td>
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<td>11</td>
<td>10</td>
</tr>
</tbody>
</table>

There are many other variants of this solution which are similar in structure. Ah! But look at the solution Clement Leung discovered using only a switch array with no VDD & GND:

For example: If \( \bar{A} = 1 \), then \( \bar{B} \) passes to \( Z₀ \), \( B = \bar{0} \) blocks move up and move down, and \( \bar{B} \) passes \( B = \bar{0} \) to \( Z₁ \).

If \( \bar{A} = 1 \), then \( B \) passes to \( Z₁ \), \( \bar{B} = 0 \) blocks move through, \( \bar{B} = 1 \) passes \( B = 1 \) to \( Z₀ \).

etc.
The 2-D Stack:

- Some errors: running straight up/down, so signal propagation doesn't occur only (data list).
- Note that inverter output goes thru clocked line into node having no other inputs active and outputs blocked by unclecked line. For example, this doesn't happen.
- Another error: cycling SHD, SHD end up shifting data right or left.
- MANY possible layouts possible. Don't know how right layout should be.

The Adder: Most people got a right answer. For details of PLA's for problems 7, 8.

However:

- Don't clock in carries unless specify context as serial adder.
- I don't check all details of PLA code, just one or two product terms - 1 output, 1 consistency. If you aren't sure of them, recheck them, I ask questions.

- Note importance of context of next level: does structure at one level not rely on rules of that level, but fit properly at the next - wrong: the "blocking of the adder."

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**FROM LAST TIME:** Pushed thru an important point. Repeat it too make sure you've noted it (Also, as you must now see - we want to get things right of to higher level before we start hooking out to inputs):

**Question:** How many minimum sized inverters will a minimum size VDD AND wire supply?

Here is 3x = 9 mm wide by 0.1 mm thick:

| ![Diagram](image) |

Have a bunch of inverters:

- VDD  | 9 mm
- 5V   | 9 mm
- GND  | 9 mm

For 4:1 inverter:

\[ R = \frac{1}{2} \times 10^4 = \frac{5 \times 10^4}{2} \]

\[ I = \frac{5}{5 \times 10^4} = 0.1 \text{ mA} \]

> Limit = 0.5 mA/mm², 9 mm wire carries ~ 5 mA

> But half are usually off

> And if 8:1, then

> But if more 8:1, like

\[ \frac{4}{1} \times \frac{1}{2} = \frac{4}{2} \text{ ten } \times \approx 200 \]

\[ \frac{4}{1} \times \frac{1}{10} = \frac{4}{10} \text{ ten } \times \approx 100 \]
BEGIN MAIN LECTURE:

AS WE'VE SEEN, CIRCUIT/SYSTEM CONSIDERATIONS OF POWER & DELAY AFFECT LAYOUT GEOMETRIES:

> WE ALMOST ALWAYS USE MIN L PULLDOWNS, FOR MIN T, BUT PULLUP LENGTH IS A FN OF RATIO CONSIDERATIONS.

> WIDER PULLDOWNS (OR PULLUPS) DRIVE LOADS FASTER, BUT ARE SLOWER TO BE DRIVEN.

YOU'VE SEEN HOW TROUBLESOME LAYOUT IS (AND THERE IS STILL ONE MORE STEP IN INSTANTIATION: LAYOUT DESCRIPTION TO GO! ... WE GET TO THAT NEXT WEEK).

> SO LET'S GO BACK AND MAKE SURE WE UNDERSTAND DELAYS IN DRIVING CAPACITIVE LOADS A LOT BETTER. ALSO, HOW TO MAKE BETTER DRIVERS. ETC

DRIVING LARGE CAPACITIVE LOADS:

SLIDE: Remember Fomont? The bigger the load, the slower it is driven.

Question: What do we do if we have a really BIG load? For example, going off-chip?

How can we drive a big $C_L$ in minimum time, starting with signal on gate of MOSFET of $C_g$?

1. Define $\frac{C_L}{C_g} = Y$.

   Intuitively, we might think to drive a larger inverter from $C_g$, then a larger one, etc., until at some point we have an inverter big enough to drive $C_L$.

2. Suppose we cascade inverters, each larger by a factor $f$.

   Then each stage has a delay of $\frac{1}{f}$, (first $f$ known) we'll see why later
3. If inter-stage delay is $T$ (or prop. to $T$ logically) then

\[ N \text{ such stages have a delay of } = NfT. \]

4. But $f^N = \frac{C_L}{C_g}$

5. If use large $f$, need fewer stages (smaller $N$) but each stage will have longer delay.
If use small $f$, need more stages, but each will have shorter delay.

\[ \text{Suppose } Y = 16, \text{ consider } f = 2, N = 4 \text{ or } f = 4, N = 2 \]

What $N$ minimizes overall delay for given $Y$?

\[ f^N = Y; \quad \ln(Y) = N \ln(f) \quad \therefore N = \frac{\ln Y}{\ln f} \]

Delay of one stage = $fT$

Total delay = $NfT = \ln(Y) \left[ \frac{f}{\ln(f)} \right] T$

\[ \therefore \text{Delay is proportional to } \ln Y \]

Figure 5 plots $\frac{f}{\ln(f)}$ as function of $f$,

normalized to its minimum value of $e$

The minimum total delay = $T$ times $e$ times

\[ \text{actual } \ln \left( \frac{C_L}{C_g} \right) \]

\[ \text{when } f = e \]
O.K. What does this mean? The implications are really quite important:

- Off-chip drivers go faster than you build up with a factor of $e$ per stage.

- But, speed isn't everything. If $h$ is off to a $f = 6$, almost as fast, but less area.

Show an [driver slide]

Discuss the whole issue of the additional Benefit To be derived from VLSI: less off-chip Boundary to cross.

[Use of inword compatible Designs; Not optimized to current chip size, to develop scalable designs for VLSI]

There will be further important uses of this simple set of ideas in the development of a Theory of the Space, time, and energy costs of computation in hierarchically organized systems. In Chapter B. pp.49-57
Super Buffers

- Ratio logic as we've seen has an asymmetry: It can discharge a $C_L$ thru its pulldown much faster than it can charge one thru its pullup.

- There are ways of getting around this problem, especially for drivers (at edges of arrays):

- Here are two circuits which approximate symmetrical in their drive capability, even though they have 4:1 $Z$ ratios:

  ![Inverting Super Buffer](image1)

  ![Non-Inverting Super Buffer](image2)

- In each case, when pulldown input to 2nd stage is $\overline{VDD}$, then the pullup gate $\overline{V}_{out}$ as in usual inverter. So pulldown the same.

- But, when pulldown input to 2nd stage goes to zero, the pullup gate goes rapidly to $VDD$, since it is only load on previous stage.

- The pulldown is turned on with $\approx 2X$ the voltage it would normally have with gate tied to source.

- Since in situation, $I \propto Vg^2$, the super buffer pulls up about $4X$ as fast as regular inverter.

- i.e., pullup/pulldown are not symmetrical. $\frac{\tau_{pu}}{\tau_{pd}} = 4$

  [This is why we got away with $T$ in the last section]
The Body Effect: We've considered $V_{th}$ to be a constant, independent of the source to substrate voltage (i.e., only a few of $V_{gs}$).

- It isn't quite that simple. Consider:

![Diagram showing the symbol for a n-channel MOSFET with $V_{gs}$, $V_{sb}$, and $V_{bias}$ labeled.]

- So, $V_{th}$ gets larger as we raise the source voltage up from ground. Comment again on $V_{gs}$, $V_{sb}$ ---

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Why Is This Increase Important?

- Because it increases 2 effects we've already introduced informally:

1. The difference in time and final output voltage between an enh. $\leftrightarrow$ dep. mode FET driving a constant load.

2. The need to increase the pull-up/pull-down $\zeta$ ratio when coupling logic stages by pass transistors.
Depletion Mode vs Enhancement Mode Pull-ups:

Depletion Mode (what we'll normally use):

- In the mid to later stages of a rising transient, $V_{gs} = V_{th}$ and $V_{gd} = V_{th}$
- So the pull-up is in its resistive region.
- The final stages of the rising transient are given simply by the exponential:
  \[ V(t) = V_{DD} \left[ 1 - e^{-t/RC_L} \right] \]
  i.e., $V(t)$ goes rapidly to $V_{DD}$, with time constant $RC_L$.
- For inverter at $0 \text{ k}$, pull-down transient $t$ and gate $C_g$, the time constant is \[ RC_L \sim KT C_L/C_g \]

Enhancement Mode
(used in early MOS)

- Since $V_{gd} = 0$, the pull-up is in saturation whenever $V_{gs} > V_{th}$
- The problem: As the output voltage approaches $V_{DD} - V_{th}$, the current supplied by the FET decreases rapidly.
- In the book, we derive: for large $t$:
  \[ V(t) \approx V_{DD} - V_{th} - \frac{C_L LD}{\mu F W t} \]

Show slide and comment
[worsened by body effect]
Pullup/PullDown Ratios For Inverting Logic Coupled by Pass Transistors.

- We found earlier that \( 4:1 = \frac{Z_p}{Z_{pd}} = \frac{L_p}{W_p} \div \frac{L_{pd}}{W_{pd}} \) yields equal inverter margins and also provides output sufficiently less than \( V_{in} \) for \( \text{input} = V_{DD} \).

- For stages of inverters coupled by pass transistors, such as:

- If input to first is zero, and thus output \( V_{DD} \). If pass T input is \( V_{DD} \), then at most the input to the second stage is \( V_{DD} - V_{thp} \).

- Since pass T source is near \( V_{DD} \), \( V_{thp} \) is near its maximum of \( \approx 0.3V_{DD} \).

Question: What must be the \( \frac{Z_p}{Z_{pd}} \) of second stage, if it is to have its output go as low with \( \text{input} = V_{DD} - V_{thp} \), as would a 4:1 with \( \text{input} = V_{DD} \)?

- With \text{input} near \( V_{DD} \), the pullup is in saturation, and pulldown is in resistive region.

compare the two equivalent circuits:
\[ \frac{Z_{p1}}{Z_{pd1}} = 4 \]

For \( V_{out1} \) to equal \( V_{out2} \), \( I_1R_1 \) must = \( I_2R_2 \).

in SAT: \[ I_{ds} = \frac{\mu E W (V_{gs} - V_{th})^2}{2LD} \] (eq 5)

in RES: \[ R = \frac{V_{gs}}{I_{ds}} = \frac{L^2}{\mu C_g (V_{gs} - V_{th})} \] (eq. 3a)

Substituting, we will find:

\[ \frac{Z_{p1}}{Z_{pd1}} \left[ V_{dd} - V_{th} \right] = \frac{Z_{p2}}{Z_{pd2}} \left[ V_{dd} - V_{th} - V_{th,p} \right] \]

Now: \( V_{th} \) of pulldowns is \( \approx 0.2V_{dd} \), and \( V_{th,p} \) of pass TS is \( \approx 0.3V_{dd} \) to 0.35 \( V_{dd} \),

**Body Effect**

\[ \frac{Z_{p1}}{Z_{pd1}} \approx 2 \frac{Z_{p2}}{Z_{pd2}} \]

(we usually either specify or measure)

\[ \frac{Z_{p2}}{Z_{pd2}} \approx 8:1 \]

Remember, think about projects a bit.

Think about what you'd like to do. Sketch out some ideas. Talk to others: would you like to collaborate? On project? Or just for checking? Any ideas others might use?