6.978. Lecture #6. Thurs, Sep 28.

- Collect Questionnaire (avail. to those who didn't get it)
- Handout HW#3 part 2 (also part 1 " " " " ")
- A few HW #1 left, handout.

- Today: (MORE RULES) Examples of layout from stick diagrams. Included will be a few more rules, and some tricks.

> Review Last Time: (Show & Discuss 3 SLIDES:)

The Si-Gate nMOS process, & the design rules.

A Little History

> Before Proceeding, reflect on diff. bet. Si-Gate nMOS & the earlier LSI process: metal-gate PMOS.

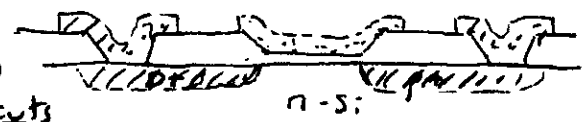
Apart from steadily increasing density as photolith & alignment & proc:

- Metal Gate has only 2 layers of interconnect Metal & Diff. While Si-Gate has 3 layers Metal, Poly, & Diff.

(Actually on ~2 1/2 since always have T where red > green)

- Metal Gate: T formed where thick oxide patterned between a metal over diff crossing? actually over a patterned gap between two diffused regions:

> Diff First placed, > Then thick oxide, (use oxide cuts to control location)



> Then cut to channel, thin oxide, cuts Then metal. [Gate not self-aligned]

- Mobility of Holes is only ≈ 1/2 to 1/3 that of electrons.

- pMOS was a much easier process to get going, for many reasons.

- So layouts in pMOS tended to be more of a hack, due to interconnection difficulties, while as we've seen, (LCD to Poly cell approach) Layouts in nMOS really have interesting topol. properties.

- Metal gate p-MOS suffered from alignment dependent large first order variations in gate-source, gate-drain capacitances due to large, variable overlap.

- Combine with lack of any consistent design methodology, you can see why LSI at first appeared uninteresting to system architects – the attitude was that such circuit and layout (Rubik) should be left to how hires & geeks. ~~However, the game has suddenly changed~~. Getting things to work was a hassle, and often required simulations of details of the circuitry (i.e., consider timing problems in unsystematically designed logic when there are huge variable capacitances hanging on everything).

- However, the game has suddenly changed. Of course most people will unnecessarily carry all the old traditions into the new game. That is fortunate for you, because they will underestimate what you can do, and will not be able to compete. (They'll think you're lucky if layout, when in fact you're mapping algorithms tightly directly in silicon structures.

→ The "Steel" ANALOGY: working a reactor melt to .001"

LAYOUT:

> Constraint on choice of levels:

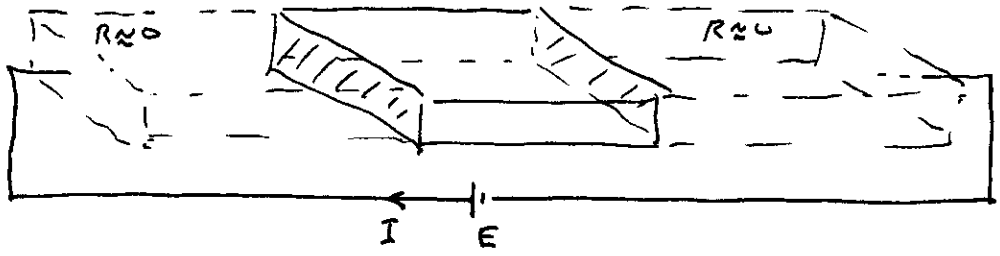
Remember we seldom have to worry about voltage dividing between wires and FETs, since wires much lower (factor of $\sim 10^3$) in resistance. Except be careful of long runs of poly that have to carry much current since poly sometimes may have $R \sim 100\,\Omega/\square$.

Poly ok for clock lines, and we'll see other long run uses later. but not O.K. for routing VDD & GND (except for short crossovers)

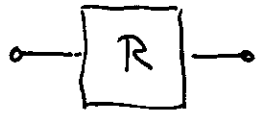
Use Metal & DIFF for routing VDD & GND.

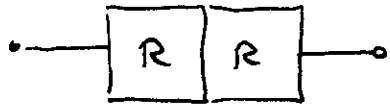
Speaking of resistances:

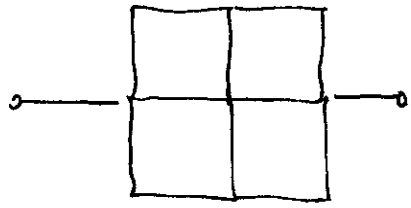
> The way I think about sheet resistivity:



Place □ between really good conductors. Measure $R = \frac{E}{I}$

So have: 

Now if did this:  $R' = 2R$

& if did this:  $R'' = R$

So, for given thickness, Resistance is same for □ of any size.

Thus we quote the "sheet resistivity in Ω/□ (ohms per square)

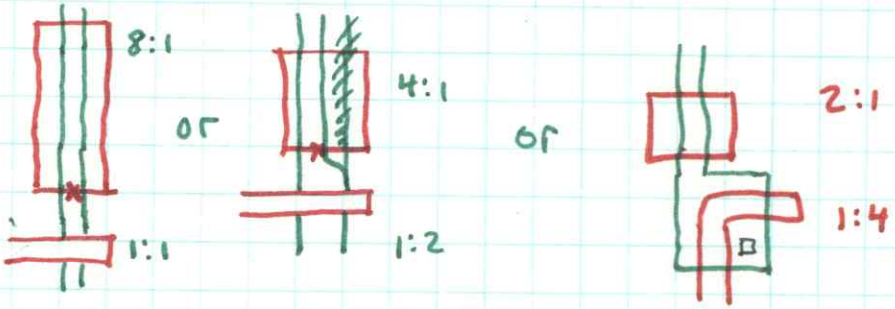
& Calculating the resistance of a layout is fairly easy: we just compute its effective L/W ratio and multiply by the sheet resistivity.

 IN DIFF, at 10Ω/□, This would have R ~ 100Ω

R_M	≅	0.1 Ω/□
R_p	~	15 - 100 Ω/□
R_d	≅	10 Ω/□
R_g	~	10^4 Ω/□

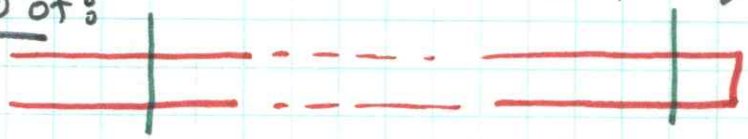
LAYOUT IDEAS: • Variety of ways to obtain any given Pullup / Pulldown Ratio:

Consider: 8:1

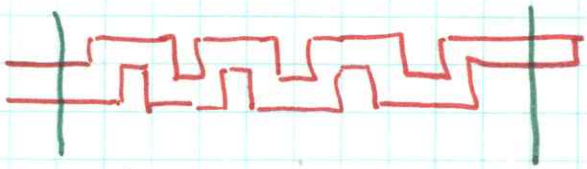


- How would you make a really big pulldown?

Instead of:

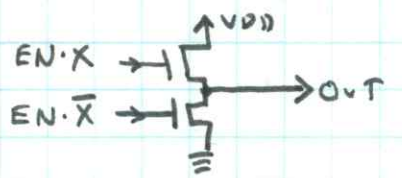


You could use a caterpillar:



(FOR GIVEN RATIO)

- CHOICE OF whether to use long Pullup / ~~narrow~~ pulldown (or) shorter pullup / wider pulldown depends on large variety of factors: (space constraints may dictate a choice)
  - > wider pulldown version consumes more power
  - > wider pulldown version drives later stage faster
  - > wider pulldown version is slower to be driven by small preceding-stage. (more next week on calculating some of this)
- EXAMPLE: IN OUTPUT DRIVER, MAY WANT REALLY BIG T's TO DRIVE OFF-CHIP CAP. LOAD: CONSIDER "TRI-STATE DRIVER":



SHOW SLIDE

(we'll use something like this only smaller in layout)

> SPEAKING OF POWER : ANOTHER LAYOUT CONSTRAINT

- We'll usually run VDD & GND to subsystems in METAL. There is a limit to how much current/unit cross section that metal can carry

- Metal migration: a phen. (not well understood) where if a current density threshold is exceeded, the metal atoms start physically moving in direction of current. If small constriction: current higher there, metal moves faster there, next thing you know it blows like a fuse.

- For Aluminum: This limit is a few times 10^5 a/cm^2 i.e. a few milliampers/μm^2

Let's use a limit in this course of 1ma/μm^2. Note the scaling we will predict shows Vertical dimension & all voltages scaling directly with the horizontal scaling. But pwr density will remain same. Thus current densities will increase.

If you want your syst. design to last a while, you might use an even more conservative value, say 0.5ma/μm^2

Unless someone finds a good way to fab high aspect ratio wires 9μm 1μm

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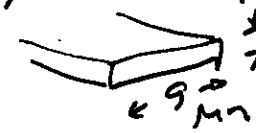
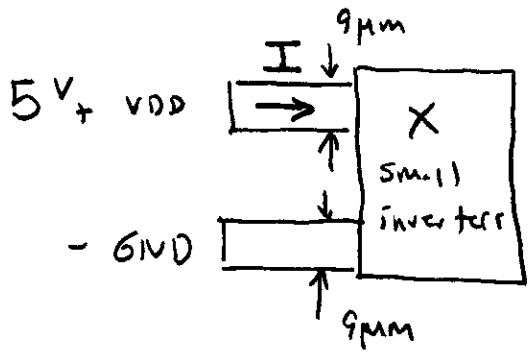
> Now what does this mean in practical terms in today's layouts

Metal Wires are 3λ wide = 9μm, and ~ 1μm thick



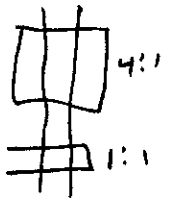
Consider the Question: How many minimum size 4:1 inverters could power lines of minimum size support?

i.e.:



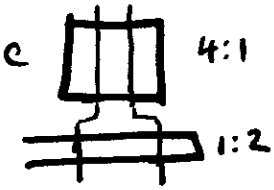
what is X when I/area = 0.5 mA ?

For 4:1 inverters: (min size) (pulldown)



ON Resistance = $(4+1)\ 10^4\ \Omega = 5\times10^4\ \Omega$

$\therefore I = \frac{5}{5\times10^4} = 10^{-4}\,a = 0.1\,ma$

- So a wire 9μ wide ~~could~~ has cross section = $9\,\mu m^2$, and can supply $9 \times 0.5\ ma = 4.5\ ma$ so **X ~ 50**
- But usually half are on, half are off so **X ~ 100**
- And if they are 8:1 rather than 4:1: **X ~ 200**
- But if make 8:1's like 

then **X ~ 100**

> WHAT THIS MEANS IS THAT MIN SIZE METAL LINES WILL SUPPLY A MODEST SIZE SUBSYSTEM, BUT NO MORE.

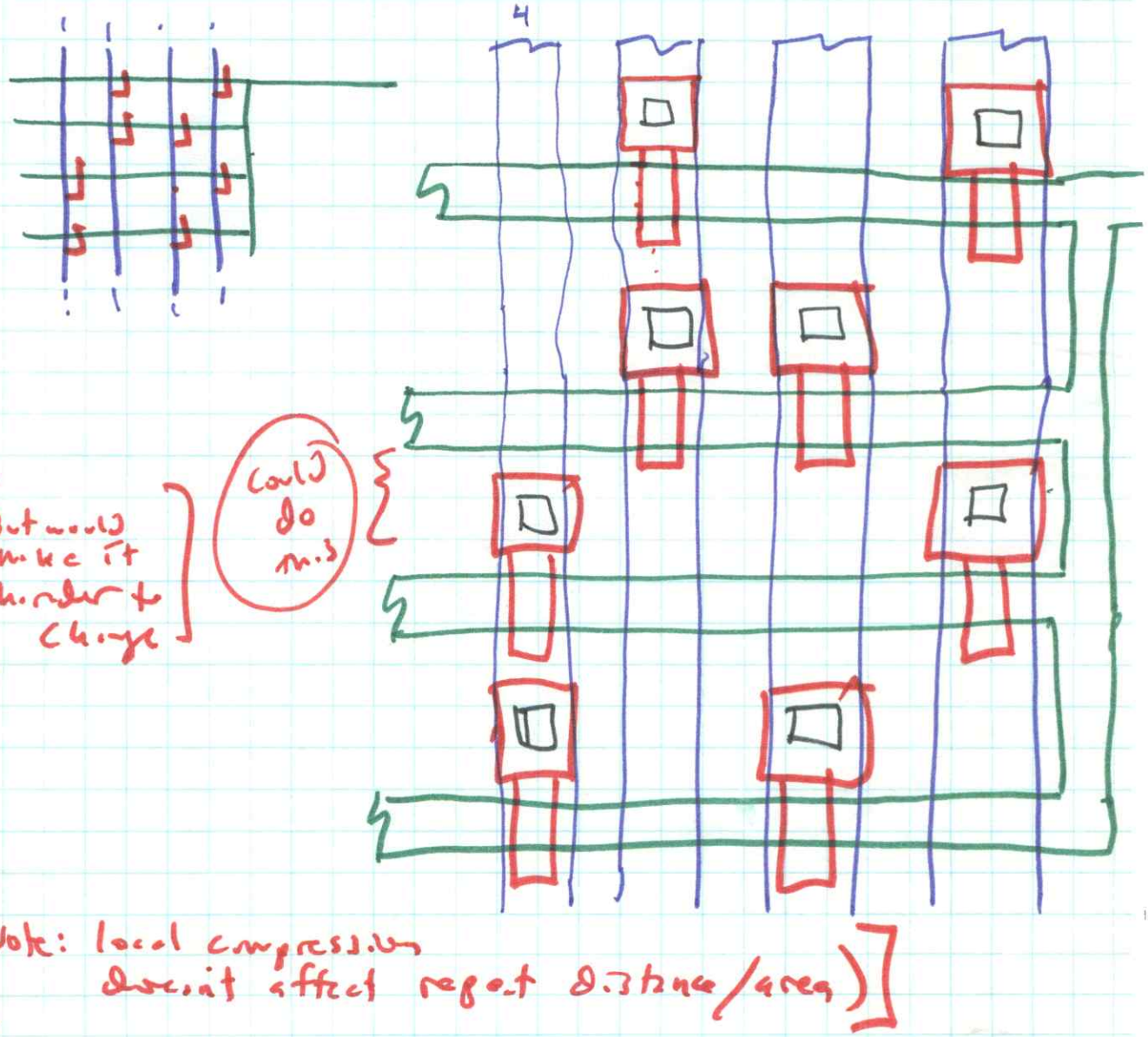
As we move up to larger subsystems, and groups of them, we at some point must start calculating the current requirements and widening the power mains appropriately:

SLIDE: FRONTISPIECE

SLIDE: CHAP 5 FIG 24

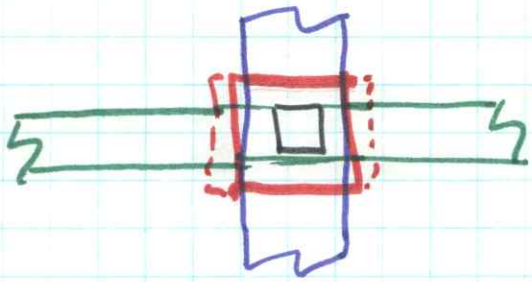
- Contribution of pass transistor to average dc power will be switching power dissipated by driving circuits at edge of arrays. (we'll go into more detail later in course)
  For now: look for pullups / shift logic
- Don't use poly or diff at these max densities. If must make crossover/crossunder use Diffusion. Widen it a bit. Keep it short. Else if >100's of diff --- it will start dropping voltage significantly.

LAYOUT EXAMPLE: on whiteboard:



[Note: local compression doesn't affect repeat distance/area]

Now note: we could do this: The rules allow:



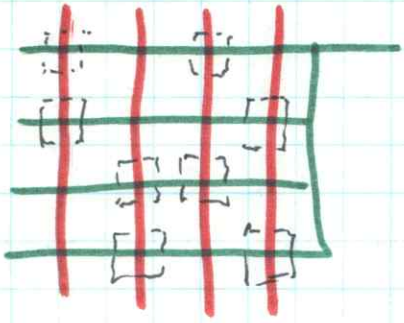
[But recommend if do this, enlarge to 1.5 to 2 lambda at edges over green]

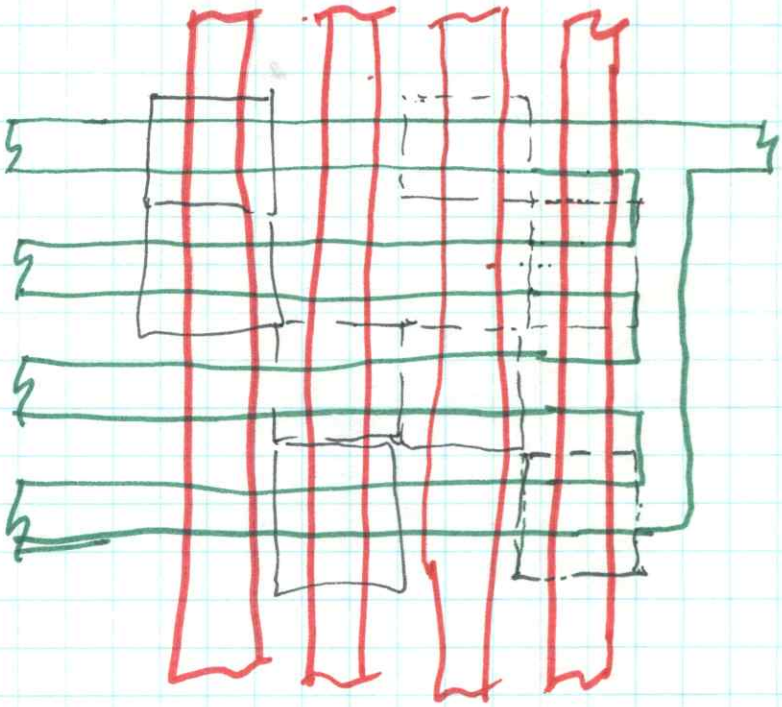
(Don't want to short out)

[Also, this may not scale well as oxide gets thinner]

- But Note: Delays get longer! No such thing as a free lunch.

LAYOUT EXAMPLE:





> LAYOUT EXAMPLE: START INTO & GO AS FAR AS CAN IN SRCELL

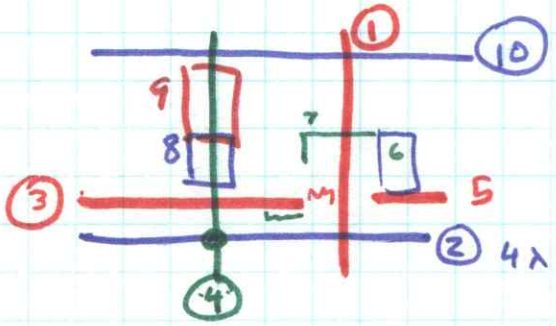
(SLIDE & WHITEBOARD)

If we're going to use a cell a lot, may want to work hard to make it small, fast, low power, etc.

But extreme compression (use of 45° lines and other ~~x~~s, AND MORE & MORE FINE STRUCTURE) CONFLICTS NOT ONLY WITH DESIGN TIME BUT ALSO LAYOUT DESCRIPTION (AMOUNT OF CODE).

[BIOLOGY ANALOGY: WANT SUBSYSTEMS THAT PERFORM FUNS USING ARRAY OF SINGLE CELL TYPE, PERHAPS SURROUNDED BY INTERFACE CELLS, ALL OF WHICH IN ADDITION TO SPEED LOW POWER ETC IS DESIRABLE IN MIN. AMOUNT OF CODE (GENES)]

WALK THRU design



Pullup/pulldown?
8:1
[what is it here: ~9:1]

A guess at min area. 3:1 pullup, 1:3 pulldown

> Now what rule makes it 21λ wide? Why but it 20λ wide?
[3λ diff-diff]

> Metal Lines could be narrower, but wouldn't make it smaller in this case. Hint at how to make it smaller
[moving cutting contact. Poss Diff]

> this version draws a bit of power. If used 16λ : 2λ pu and 2λ : 2λ pulldown, would use ~1/3 power

But would have longer pu transit time, and wouldn't drive outputs as fast, but would be less load on inputs.

> Actually might not be much bigger — might be able to angle the pullup around a bit

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> If have time (unlikely), could start PLA cell layout.

EXPLAIN/CLARIFY HW #3 problems 10 and 11

i.e. read carefully to identify constraints given and constraints not present

[Sketch layouts as in Fig 86 chap 4
SHADE IN COLORS LIGHTLY
IF you want to apply another constraint do so but state it!
(SHOW SLIDE OF TOPOLOGY OF STACK
[SUGGEST TRACING DIRECTLY MIRRORED CELL TO CHECK CELL-CELL DESIGN RULES]