TODAY: • The Si-Gate nMOS Process
• Layout Design Rules

THURS: • Examples of Layouts, From Stick diagrams.

LECT: SEP 26

LECTURE #5 (TUES)

Admin • Handout Homework #3 ←
• Handout Questionnaire
• Collect Homework #2

A (start over) x,1/0; 1,0/0; 0,0/0; 0,0/0; C; B; D ...; even #1s; 1,0/0; odd #1s; M,R/E

• Announce: New Room, St. next time: 39-400

• Explain Questionnaire: Lab sched / Poss. Seminars.

Discuss HW #1:

• Most did very well. If have questions, see me.
• Show best solution to #2(a) - J. D. Brooks, several others had similar solutions. (ON BOARD)
Interesting thing: Area goes linearly with # inputs. Solution I'd shown before, and those that most got, went as N^2.

Anticipate next week's lectures

• Show 2 versions of Selector. Indicate what's to come in delays in pass transistors is $\propto n^2$. So, not too many of these: They simplify/compact layout, but add delay.

• So, there are real limits to how far we can carry the neat "arrays of pass transistors" idea. We'll get more into this next week.

• Note: Already hinted that if couple inv. logic with pass transistors, then must use 8:1 pullup/pulldown ratio. Why?

VDD, VDD, VDD, V_{IN}, V_{out}

$V_{IN} \leq VDD - V_{TH}$

We'll calculate this more next week

VDD is highest voltage. If VDD on gate of pass-FET, then V_{IN} can at most be $VDD - V_{TH}$. So, for VOut to go as low with $V_{IN} = VDD - V_{TH}$, as would normal inverter with $V_{IN} = VDD$, must have higher ratio

- Bring this up now because: Some people used depl mode pulldowns & enh mode pullups. This was o.k.: given info you had. But be careful:

VDD — VDD

Suppose want a non-inverting level restoring stage: If input = VDD, output at most = VDD - Vth.

If you keep going, each stage would have lower output. As we'll see, such a stage would be very slow also.

- All this points out we must look a little closer at our basic circuits, their delays, etc. (Next week) Before we go wild stick diagramming.

3(C): More switches. Some thought it very interes., some went on to find PLA constructions

Note: There are no best solutions. It all depends on context, and what constraints are imposed by next higher level.

The Silicon-Gate Process: • Overview. Then Intro to

- Patterning: Now we're going to look closer at our PCB technology. At the steps in the process of building up the layers. From this we will develop the ideas on which the layout design rules are based. We'll somewhat abbreviate/simplify the description today — but still cover the essentials. We'll talk a bit more later in the course about the details of the present day process we'll actually use.

- Overview: (Slide from Ch. 4) Talk Thru Slide
  Archit. - Des - Sticks - Layout - Des Layout then
  MAKE THE MASTER PATTERNS FOR EACH LAYER (MASKMAKING)
  & then Transfer these into each layer at approp. process step (wafer Fab)

Hold up Artifacts: MASK. WAFER.

- We'll come back to how to describe layouts, and make masks later. We need to develop the geometric rules for generating layouts before we can have any to describe.

  We deduce these rules from an understanding of the process of patterning (with masks) during processing

- PATTERNING: There will be 5, or 6, (or sometimes more steps) involving transferring a mask pattern into a layer during processing.

  Rather than repeat the details of this each time, lets go thru it once, and then go on to describe the particular sequence of layers patterned without repeating all the details of the patterning itself.

- So How is a mask pattern transferred into a layer. Probably the classic case is the patterning of SiO_2. This is done several times during the nMOS process.

Talk Thru 2 SLIDES. Maybe use Board.

> Oxide grown (expose bare wafer to O_2 in furnace) on silicon wafer.
> Coated with a photo resist material: a particular organic compound.

> 2 kinds of resist: Positive (UV light [ionizing radiation]) breaks it down.
> Negative (") hardens it.

> Let's use positive example here: Place mask at or near surface, expose

> Wherever radiation passes thru openings in mask, it enter the resist, SiO_2, Si. No effect on SiO_2, Si. But, breaks down resist.

> Develop it in organic solvent which rapidly dissolves broken down resist (but only very slowly attacks other).
> Now we use a selective etchant in this case HF, which dissolves SiO_2 but not resist and not Si.

> Use stronger organic solvent to remove resist.
> Have transferred the Opaque Mask pattern into SiO_2 (Positive)

(MORE CONCERNED NOW WITH CHARACTERISTICS OF STRUCTURE CREATED Rather Than ALL Detailed Steps)

- Now: Let use a slide sequence to get a 3-D view of the nMOS process sequence, looking at just the vicinity of one enhancement mode MOS-FET: **GO THRU SEQUENCE.**

  > [Note use of Negative resist in the first case shown, i.e. Compl. of opaque pattern is transferred into the resist.]

  > [Note missing one mask. We'll come back to that later when we look at sequence covering a more complex structure which contain Depl.-Mode pullups]

  > Emphasize That This is going on everywhere across wafer at same time. The process steps are Pattern Independent. It's like Developing Film.

- Now: Lets take a look at a single slide which contains a great deal of info: Shows the entire Sequence and details of profile of a more complex structure: an Inverter, being built up as successive process steps occur. **TALK THRU SLIDE.**

  Be sure to mention:

  > thin oxide regrowth before poly is put down (Fig 11)
  > note how Poly blocks diffusion (Fig 12)
  > Contact cuts only go just so deep.
  > Metal over cut to poly next to diff: Butting Contact more later

  > Mention Sixth mask: Overglass & then cut to Pads

- Mention That most books/articles concerning the process show these profiles. We usually don't need to see these. Ph: and there aren't many books that show the other view yet.

LAYOUT DESIGN RULES

Now we've gotten enough of an idea about the process to develop a set of rules which describe permissible layout geometries.

- What are major problems in the process? **FOR GIVEN PROCESS:**

>> There is some standard deviation in line-widths

$$\sigma = \sqrt{\overline{(X-\bar{X})^2}}$$

$$\sigma = \sqrt{\frac{\Sigma(x_i - \bar{x})^2}{n}}$$

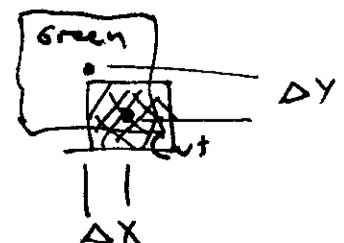
> If make them too small, they'll sometimes disappear!

> If put them too close together, they'll sometimes touch!

>> There is some standard deviation in interlayer registration

(We haven't said how these are re-registered yet. We will later in course. But you can see the problem)

For example: a contact:



- These deviations are typically of the same order, i.e. not economically useful to have one << the other. They are being pushed down together.

- Normally, there is known for any given FAB Line, a minimum line width / line separation. This is an <u>empirical value</u>: if you try to make lines smaller/closer, you'll get into trouble.

- We define the <u>half-width</u> of the minimum lines as the <u>length unit λ</u>. for the particular process

  minimum width lines — λ

- <u>Think of λ as</u> some moderate # multiples of the standard deviations σ_w and σ_r.

- <u>Think of λ</u> as the "resolution of the process"

[We will develop the set of design rules in dimensionless form : i.e. as a set of ratios of permissible geometries to the length unit λ]

- These rules will have some reasonable longevity. They've been "designed" with future scaling effects in mind. At any time on any particular Fab line, some of the rules individually may be weakened leading to denser layouts.

- <u>However</u>: We prefer for prototyping, teaching, communicating ideas, to have a standard single set of rules which will last a while. Designs done with these rules can simply be scaled down to be run on future fab lines.

- <u>For a product</u>, in highly competitive market, you will likely do further optimization to the detailed rules of the manufacturing Fab line.

The Rules:

SHOW SLIDE: RULES,

- As said, take as given some min. line half-width.

> So Fig 15 Min diff line = 2λ
> Fig 23 " poly line = 2λ

> Min Sep is same: min poly sep (Fig 18) = 2λ

> But We usually use min diff sep (Fig 16) = 3λ
since if high voltage of these, if too close, their depletion regions may overlap and current flow between them.

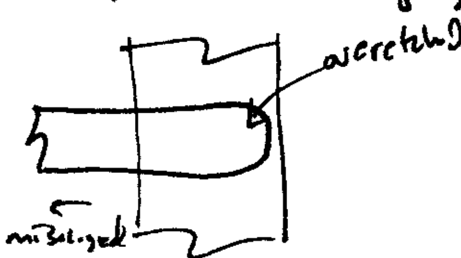
Note: Some processes use a special step to eliminate this problem.

> Now: What about two level separations:

Fig 19: Must keep at least λ bet. poly & diff (unconnected) or will get an unwanted large capacitance when red overlays green

> Fig 20: When Form a transistor (poly over diff)

Must overlap by at least 2λ. Reason, if ever there is not an overlap, will get a short circuit



An EXAMPLE OF SPECIAL RULE: [If poly width > $n\lambda$, then overlap can be $\geq 1.5\lambda$]

Continue with Slide 1

- Fig 21 shows examples: overlap Poly 2λ, poly-diff sep 1λ, diff must be 2λ wide (tricky one)

- To Form Depl. mode FETS: Yellow region must extend 1.5λ beyond gate. & must be $1.5\lambda^+$ from any enhancement mode gates. Fig 22

- Contacts: See Figures 23, 24, 28.

  > Cuts must be min. linewidth size: min = $2\lambda \times 2\lambda$ square

  > Must be surrounded by at least one λ on all sides, to insure contact, and no contact with unwanted layer

  > Cuts to diffusion must be 2λ from nearest gate to positively insure no shortout of FET

  > usually use many small cuts to contact large area of diff, which decreases contact resistance.

Fig 27/28
- METAL: Due to Steep Slopes, rough terrain, Metal Should be 3λ wid 3λ sep (except contacts o.k. 1λ)

- BUTTING CONTACT: If want to Contact Red to Green, use Butting contact (describe)

(if time)

- Buried Contact: There is another way. We sometimes use it, but don't recommend it in general. With another mask step, can cut the thin oxide in selected regions prior to putting down poly, and then special sequence (then fab line) can make direct poly-diff contact. Rules are very fabline dependent.
  Advantage: much smaller contact area. Can run indep metal over top. Makes some layouts much more compact

---

- In principle can contact to Poly over Gate: But, can't do this to minimum size gate especially if have 2λ on all sides.
  Draw sketch