LECTURE #3: 19 SEPT:

- Pass Out HW #2 (a)
- Hand In HW #1
- How Many Think They found a reasonable solution to Prob. 2(a)?
- Are you interested in seeing a solution? Stick Diag, Dicks Soln. [Put on White Board ?]

Where we are:

This Week We Move Up a Level:
- Discuss Inverter Delays & a clocking scheme. Then:
  - We'll learn how to make Registers.
  - We'll study an example subsystem: A Stack
  - We'll learn how to impl. irreg C/L in a regular way using PLAs
  - We'll learn how to implement Finite State Machines using registers & PLAs.

Next Week We Move down a Level:

- Study the Silicon-gate nMOS process.
- Based on that, we'll develop a set of Design Rules which constrain how close we place wires, how narrow they may be, etc. (Geometrical Constraints)
- These Design Rules + rules based on the electrical property of FET's and wires (such as the 4:1 rule) will determine how we may layout our stick diagrams.
- We'll look at some example layouts
**Inverter Delay:**

- **Resistive Region:** \( T = \frac{L^2}{\mu V_{ds}} \)
- **Saturation Region:** \( T = \frac{L^2}{\mu (V_{gs} - V_{th})} \) [larger \( V_{ds} \) doesn't reduce \( T \)]

- Examine case where an inverter drives several similar inverters:

  - Suppose: \( V_1 = 0 \). Then at \( t = 0 \),
    - Drive \( V_0 \rightarrow V_{DD} \).
    - What happens?

**Graph of Effect:**

- IT takes \( n\tau \) (mean) to remove the "positive charge" from the \( C_g \) of the second stage - then the pulldown of the identical first stage.

- When second stage turns off, 3rd stage \( C_g \) charges up (from pullup of 2nd) to \( V_{DD} \).

- BUT pullup has less current capacity than pulldown, so the charging up takes longer, by \( \sim \) ratio \( h = \frac{2\rho_0}{2\rho_0} \).

- So normally speak of inverter pair delay = \( (1 + h)T \).

- If Fanout \( f \) (i.e. 1st feed \( f \) next stages in \( U \)) or if next \( C_g \) is larger by factor \( f \), then multiply switching delay time by factor \( f \).
Some Approx Values in 1978

- Small FET's have gates 6 x 6 µm

- Resistances
  Metal ~ 0.1 Ω/µ, Poly ~ 15-100 Ω/µ, Diff ~ 10 Ω/µ
  Transistors: 10^4 Ω/µ  
  Note: Res FETs >> Res wires

- Capacitances: (to substrate)
  Metal 0.3 × 10^{-4} pf/µm², Poly ~ 0.4 × 10^{-4}, Diff ~ 0.8 × 10^{-4}
  Transistor Gates: ~ 4 × 10^{-4} pf/µm²
  Note: Cg only x10 that of wires. But wires typically x10 area of gate they feed. So typically must multiply X 2 the gate capacitance to estimate delays. (Call this parasitic capacitance)

- Calculate ∆ Two ways: (Ballpark, to get order of magnitude)

> \[ \tau \approx L^2 / \mu \left( \frac{VDD}{2} \right) \]  
  Now 800, \( n = 800 \) cm²/volt-sec  
  \[ \tau \approx \left( 6 \times 10^{-4} \right)^2 / 800 \]  
  = 0.39 × 10^{-9} = 0.39 ns  
  So actual inverter ∆ (incl. x2 for parasitic) = 0.36 ns

> \[ \tau \approx R_{FET} C_g \times 2 \text{ parasitic} \]  
  \[ \tau \approx 10^4 \times 4 \times 10^{-4} \times 10^{-12} \times 2 \times 36 \text{ (nm)} \]  
  \[ \tau \approx 288 \times 10^{-12} \approx 0.29 \text{ ns} \]

- Above are actually what we would mean for ∆ in R/C oscillators for the best current 6 µm processes. Over many processes, typically \( 0.3 < T < 1.0 \) ns
**Notation:** You've read about Notation. In particular, Mixed Notation

While not formalized, yet will be very useful. Will become clear by example. Useful to

1. Reduce clutter in diagrams. Parts of less detailed interest can be left in higher level form.
2. Diagram designs when only some of the details have been derived and/or known.

**Two Phase Clocks:** START OVER ON 88

We will use one particular clocking scheme to determine times when we'll allow data to enter and update the contents of registers in our systems:

We call it: Two-Phase, Non-Overlapping clocks

Let's plot the clock signals as for(t):

\[ \phi(t) \quad \phi_2(t) \]

The signals switch between 0 and \( V_{DD} \).
Both have the same period \( T \).
The high times of both are shorter than their low times.
They are never both high at the same time, i.e. they never overlap.

**What the clock meters must never, never do:** Open

- Timing/Synchronization are in the general case subtle, complex. We'll come back to this later. For the simple system in synchrony, the 2-8 is perfectly okay.
THE SHIFT REGISTER:

- Perhaps the most basic structure for moving a sequence of data bits. It is the basic structure from which we will derive our notion of "Registers" and R-R Transfer

- Draw circuit diagram:

- Describe movement of data during \( \phi_1 \) followed by \( \phi_2 \)
  
  (Mention term "pass transistor" or "transmission gate").

  As these transistor "switches" not part of pull-up/pull-down
  static logic, i.e. they lead to effective loads only, not VDD or GND

- Now show alternative diagram: mixed notation:

- Describe: especially; Must envision the input of the
  inverter as leading to \( \text{\textit{CG}} \), the gate of a FET.

- Now start to show part of stick diagram:
\[ \phi_1(t) \]
\[ \phi_2(t) \]
\[ X(t) \]
\[ V_1(t) \]
\[ V_2(t) \]
\[ V_3(t) \]

\[ V_1 \rightarrow V_3 \quad \text{in} \quad T = \phi_1 + \phi_2 \]
Continue to Build on Shift Register Idea:

How could we move a sequence of words from register stage to register stage—rather than just a sequence of bits?

- By stacking together several shift registers in parallel, as follows:

- But this is just moving data around. How do we control the data movement? Ah! By putting some switching or C/L function in between register stages:

An example: Shift up / straight thru register stage:

(FLIP OVER TO VG SCREEN)
- Diff levels of abstraction simultaneously present. How to visualize function of successive INV Logic stages Sep. by pass transistors?

  Show & Discuss Fig 6 Slide

- How to impl simple registers:

  Show & Discuss Fig 7-9 Slide

- Design of a stack subsystem (Intro: to be cont. next time)

- Talk thru basic idea:

  Design of a stack subsystem

  Push

  Stack

  Word size in bits

  Pop

  # words

  Deep

- First conceive of a cell design for one bit of one track:

  SHR.φ₁

  TRL.φ₁

  Follow bit thru various φ₁-φ₂ possible cases

  TAR.φ₂

  SHL.φ₂

- Show slide and discuss layout (or sketch)

- Show controller chip slide.

  (Will see how to complete the overall subsystem design next time, incl. gen. the CTL signals)