LECTURE #2: 14 SEP

WHITEBOARD: EXAMPLES OF LECT 1, FOR THOSE WHO WISH TO TAKE NOTES WHILE BOOK IS HANDED OUT.

HAND OUT BOOK: EACH STUDENT REGISTERED FOR THE COURSE SHOULD GET ONE. YOU SHOULD BE ON THIS LIST. PLEASE SIGN BY YOUR NAME SO I'M SURE YOU GOT YOUR COPY. DON'T LOSE IT

GO OVER BOOK: SINCE LACKS INDEX, ETC., LET ME DESCRIBE HOW ORGANIZED

> ORGANIZED INTO 4 MAJOR SECTIONS. 1,2 / 3,4 / 5,6 / 7,8,9
> WE'LL COVER MOST OF CH 1-4 STUDY EX IN 5-6
> A BIT ABOUT THE BACKGROUND OF BOOK.

> A BIT ABOUT THE BACKGROUND OF THIS NEW FIELD OF ACTIVITY AS A VERY COLLABORATIVE EFFORT OF A NUMBER OF PEOPLE IN MANY COMPANIES & UNIVERSITIES. SO YOU SHOULDN'T ENVISION THIS AS JUST AN ISOLATED NEW COURSE. IT IS PART OF A YET LARGER "SYSTEM", A CONTEXT I HOPE TO TELL YOU MORE ABOUT AS WE PROCEED.

> I ALSO HOPE TO HAVE SOME OF THE OTHERS VISIT HERE. THERE MAY BE AN INFORMAL OCCASIONAL SEMINAR.

> I HOPE TO HAVE PROF. CARVER MEAD VISIT WITH US IN DECEMBER AND GIVE TWO LECTURES ON TOPICS OF CURRENT RESEARCH ACTIVITY: HIGHLY CONCURRENT SYS. & PHYS. OF COMP SYS.

HANDOUT REST OF HW#1. Clarify HW#1.

> FOR EXAMPLE: Clarify function to be implemented in Problem 2(a).*

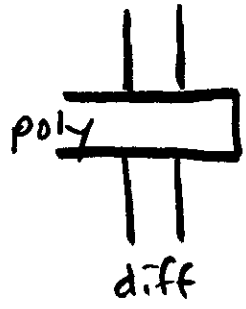
> Mention again: Some problems* will require design, even invention. In such cases only a small fraction of students may get an answer---

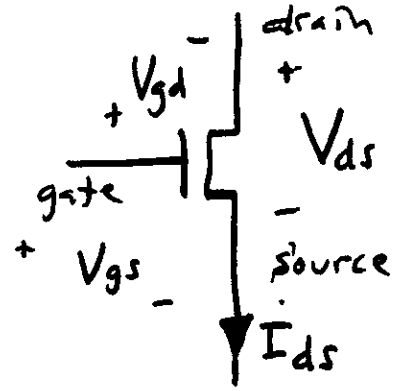
NOW, IN 50 MINUTES: INTRO TO MOS TRANSISTOR AND BASIC LOGIC CIRCUITS COMPOSED OF MOS-FETS

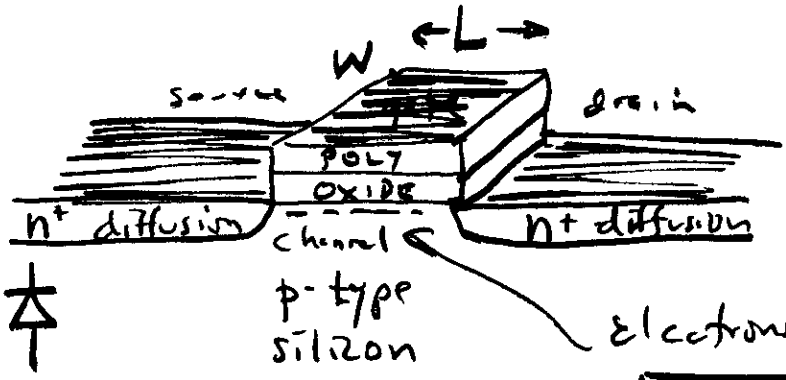
FOUR TOPICS: AND THESE ARE ALSO ASSIGNED READING IN TEXT.

> The MOS Transistor
> The Basic Inverter
> Inverter Delay
> Basic NAND/NOR Logic Gates

MOS TRANSISTOR: Put up ViewGraph

① 

② NAMES/SYMBOLS 

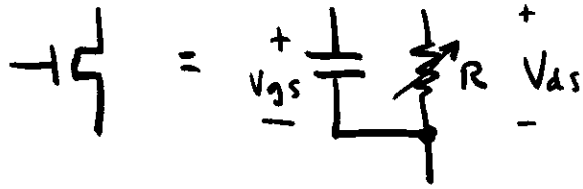
③ 

electron attracted if $V_{gs} \geq V_{th}$

Enhancement Mode if $V_{th} > 0$

- $I_{ds} = Q / \tau$
- $\tau = L / \bar{v}el = L / \mu E$
- for small V_{ds}, $E = \frac{V_{ds}}{L}$ $\therefore$ $\boxed{\tau = \frac{L^2}{\mu V_{ds}}}$
- Transit time is the fundamental time unit of our intrinsic system. All times scaled to τ of smallest FETs in system.

- Neg Q in transit $= -C_g(V_{gs}-V_{tn}) = -\frac{\varepsilon WL}{D}(V_{gs}-V_{tn})$
- $I_{ds} = -I_{sd} = \frac{\mu\varepsilon W}{LD}(V_{gs}-V_{tn})V_{ds}$
- For given $(V_{gs}-V_{tn})$, $I_{ds} \propto V_{ds} \Rightarrow$ 

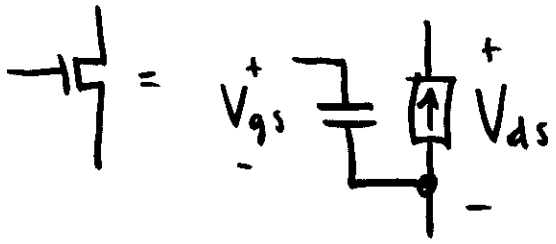
i.e. 

∴ For small V_{ds} & $V_{gs}-V_{tn}>0$ } Resistive Region

$$V_{ds}/I_{ds} = \text{"}R\text{"} = L^2/\mu C_g(V_{gs}-V_{tn})$$

- As V_{ds} increased so $V_{gd} < V_{tn}$, i.e. $V_{ds} \geq V_{gs}-V_{tn}$

Transistor enters saturation region. Further increases in V_{ds} neither increase current significantly nor decrease T

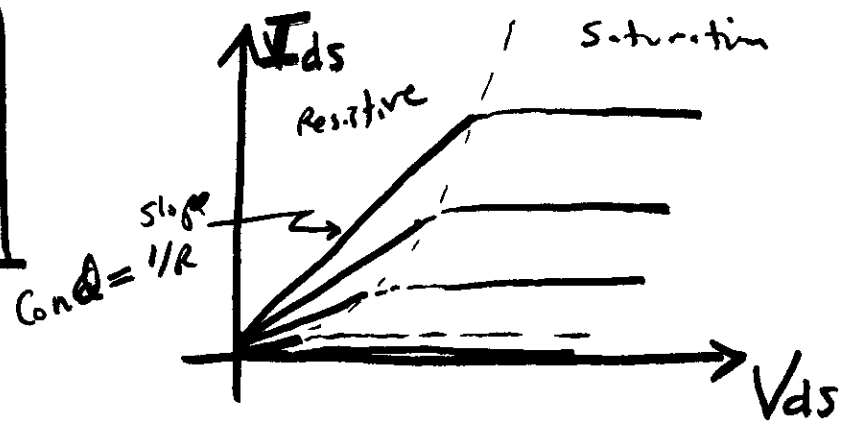


$$I_{ds} \cong \frac{\mu\varepsilon W}{2LD}(V_{gs}-V_{tn})^2$$

} In Saturation, FET behaves like current source controlled by $V_{gs}-V_{tn}$

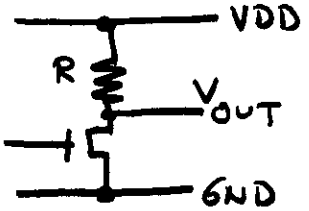
∴ Transit time is $T = L^2/\mu(V_{gs}-V_{tn})$

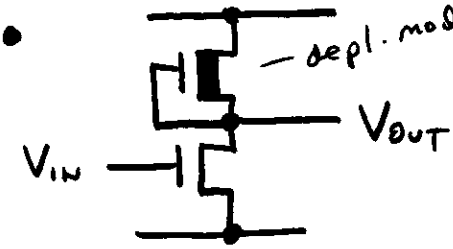
Draw & Discuss Characteristics Summarizing These Regions



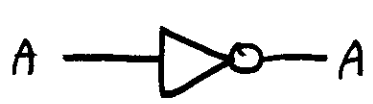
THE BASIC INVERTER: PUT UP SLIDE 2

- FCN: OUTPUT TO BE COMPLEMENT OF INPUT
- WHEN DESC LOG FCN: LOGIC-1 ≡ VOLTAGES ≥ Defined Logic Threshold
  LOGIC-0 ≡ " " < " " "
- If could make resistors, could build inv.:
  explain function
  But, R's especially of high value, long wire.



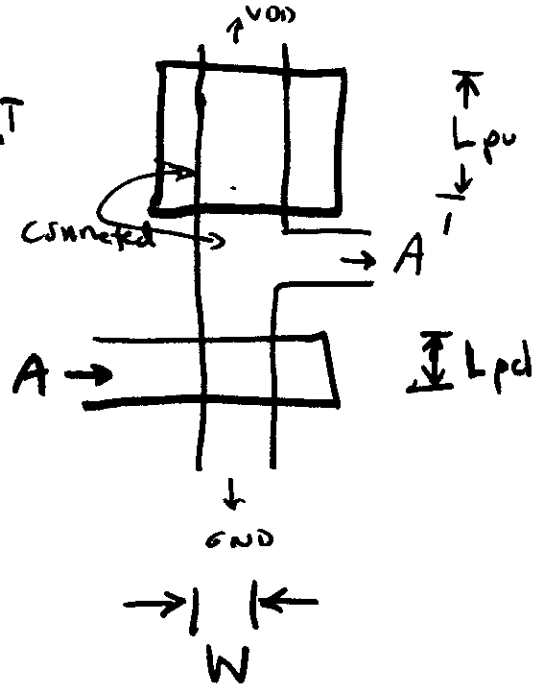
- so, We use a depletion mode MOSFET in place of a resistor
- The depletion mode MOSFET has a threshold voltage Vdep that is less than zero. During Fab ---
- 

depl. mode ⟷ with gate tied to source, $V_{gs}=0$, ∴ ON

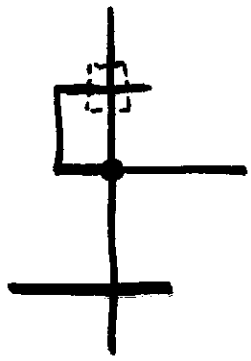


A	A'
0	1
1	0

- LAYOUT



- STICK



- For Reasonable ratios of $\frac{L_{pu}/W_{pu}}{L_{pd}/W_{pd}}$,

INPUT VOLTAGES ≥ A DEFINED LOGIC THRESHOLD VOLTAGE V_{INV} WILL PRODUCE OUTPUT VOLTAGES BELOW THAT LOGIC THRESHOLD VOLTAGE & VICE-VERSA.

- Figs 3a, 3b show characteristics of a typ pair of MOS Transistors used to impl. inverters

The relative locations of saturation differ due to the differences in threshold voltages.

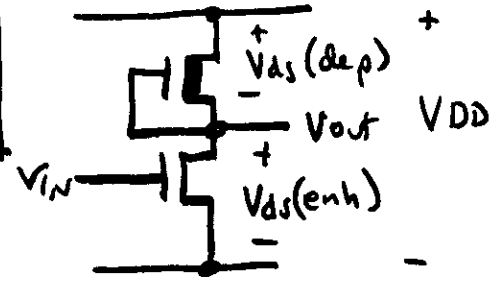
CALCULATE INV. TRANSF. CHAR: i.e. V_{out} vs V_{in}

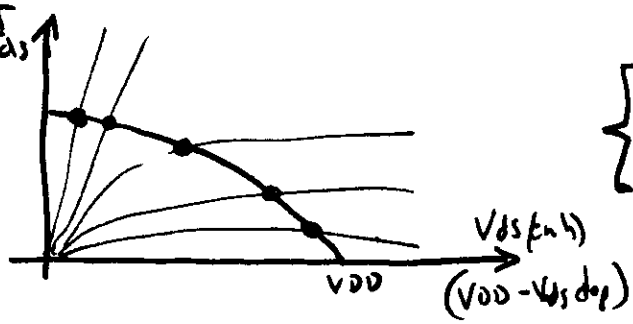
- Rather than back away at solving equations - lets use a graphical construct to determine the transfer characteristics of an inverter composed of 2 such transistors. We usually don't have good analytical expressions for characteristics anyways - just measured curves.

SLIDE

- $V_{ds}(enh) = VDD - V_{ds}(dep)$

Also: $V_{ds}(enh) = V_{out}$



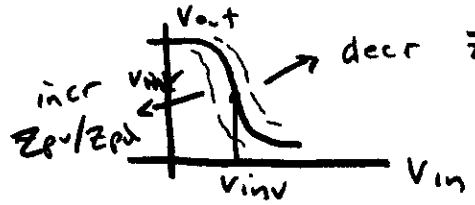
- 

{ only one curve for Depl Mode FET is relevant: That for $V_{gs} = 0$

Superimpose
$I_{ds}(enh)$ vs $V_{ds}(enh)$ (VS)
$I_{ds}(dep)$ vs $(VDD - V_{ds\,dep})$

Since currents equal, intersection of curves yields

$V_{ds}(enh) = V_{out}$ vs $V_{gs}(enh) = V_{in}$

- 

|slope| = Gain

INVERTER LOGIC THRESHOLD VOLTAGE

Logic threshold $\neq V_{tn}$ of the enh. mode FET

V_{INV} is that V_{IN} which yields an equal V_{OUT}

ITS VALUE DEPENDS ON RATIO OF

Z_{pu} to Z_{pd} i.e. $\frac{L_{pu}/W_{pu}}{L_{pd}/W_{pd}}$

(Read in Book) we find $V_{INV} \cong V_{TN} - \frac{V_{dep}}{\sqrt{\frac{Z_{pu}}{Z_{pd}}}}$

- To maximize $V_{gs}-V_{th}$ and increase pulldown's current driving capability, V_{TN} should be as low as possible. But if too low, inverter outputs won't be driveable below V_{TN}.

Typically $V_{th} \cong 0.2 VDD$

- To maximize pullups current driving capability, might set V_{dep} for negative. However, for given V_{inv} & V_{th}, decreasing V_{dep} requires increasing L_{pu}/W_{pu} → typically requiring more area.

Typically $V_{dep} \cong -0.8 VDD$

- In general, desirable to have equal margin around the inverter threshold i.e. that

$V_{INV} = VDD/2$

- .2 & -.8 choices → $V_{INV} \sim \frac{VDD}{\sqrt{\frac{L_{pu}/W_{pu}}{L_{pd}/W_{pd}}}}$
- ([illegible]) This leads to a pullup/pulldown ratio of

$$\frac{Z_{pu}}{Z_{pd}} = 4:1$$

INVERTER DELAY

Look at the delay thru a sequence of inverters: this is the simplest case for estimating delays.

Define $k = Z_{pu}/Z_{pd}$: Use alt.  symbol.

See figure 4a **SLIDE**

- AT T=0, STEP VDD ONTO INVERTER 1, & LOOK AT WHAT HAPPENS.
- WITHIN ~ τ, pulldown of 1st remove $Q \approx V_{DD} C_g$ from gate of second inverter.
- Pullup of second must supply this charge to C_g of third, but it can supply only about 1/k'th the current of pulldown of 1st.
- So speak of inverter pair delay (one ~~low~~ going / high going transition)

$$\text{inverter pair delay} \cong (1+k)\tau$$

- If one inv drive more than one succeeding (identical) inverter, for example f of them,

  then delay of both up and down transitions is simply increased by a factor f_g for a fanout of f

- These simplified notions of delay are based on a "switchy" model where individual stages spend only a small fraction of their time in the mid-range voltage values near V_{inv}

NAND & NOR LOGIC GATES

- These are constructed as simple expansions of the Basic Inverter Circuit.
- Their behavior, logic threshold voltages, transistor geometry ratios, time delays also direct extensions of the analysis of the inverter **SLIDE**
- Discuss figures 6a thru 6c
- Note that the logic threshold of the NAND is given by

$$V_{thNAND} \sim \frac{VDD}{\sqrt{\frac{L_{pu}/W_{pu}}{n\, L_{pd}/W_{pd}}}}$$

so Z_{pu} must be bigger (L_{pu} longer) than in inverter

- Also, $T_{NAND} \sim n T_{INV}$, and both up/down delays longer.
- So, while NAND is easy to "stick" into circuits, it has very poor area & delay characteristics. Be careful in its use in "real" designs.
- **STICK DIAGRAM NAND & NOR GATES**
- **QUESTIONS?**