LECTURE #14 NOVEMBER 7

- TODAY: REVIEW EXAM; EFFECTS OF SCALING
  GLEN: CELL LIBRARY
- NOTE: PROJECT ASSIGN #2 DUE THURS. PLEASE HAND IN XEROX COPY SO I CAN KEEP YOUR DET. PROJ. DESC. FOR REFERENCE

  TIME IS MARCHING ON. ANYONE WHO HASN'T GOT A PROJECT IDEA BY NOW SHOULD MAKE AN APPT TO SEE ME – I'LL HELP SELECT AN IDEA.

BY THE WAY: GOOD NEW RE PROJ. SET IMPL.

- NOTE: ON NOV 21 (TUES) DICK LYON OF XEROX PARC ~~[illegible]~~ WILL PRES A SEMINAR ON VLSI IMPL. OF SPEECH PROCESSING FUNCTIONS.

  HE WILL PRES. SOME BASIC BUILDING BLOCKS ADDERS, MULTIPLIERS, MEMORY SUBSYSTEMS, OUT OF WHICH ONE CAN BUILD A DIG. SIGNAL PROC. SYSTEM. HE WILL THEN DISCUSS AN EXAMPLE PROJECT CHIP NOW IN DESIGN: A N30 CH ~~ALL~~ DIGITAL BANDPASS FILTER BANK WHICH WILL FIT ON ONE CHIP EVEN IN PRES. TECHNOLOGY.

  HE WILL GIVE A PRES. OF THE OV. SYS. DES OF AN ISOLATED UTTERANCE RECOGNITION SYS. WHICH SHOULD FIT ON ONE OR A FEW CHIPS WITHIN A FEW YEARS. (FOR VOICE INPUT TO COMPUTERS)

- NOTE: CALVERT MEAD OF CALTECH WILL PRESENT A SEMINAR ON HIGHLY CONCURRENT SYSTEMS (CHAP 8 MAT'L) ON TUESDAY DEC 5.

[TRY TO HAVE LEVITT, TODD, TAKE EXAM DURING CLASS.]

- LETS REVIEW THE EXAM: HAND-OUT GRADED EXAMS

- THE MEAN = 80, MEDIAN = 86
  HIGHEST GRADE = 96 (2 people: GUY STEELE, MOSHE BAIN)

- 11 between 90-96
  9 between 80-89
  10 below 80

MOST DID VERY WELL. CONSIDER OVER 80 AS A GOOD GRADE.

REFER TO EXAM SHEETS:

I GRADED FAIRLY HARD. A FEW WHO HAVE DONE VERY WELL ON HW DID POORLY. MAYBE HAD A BAD DAY. DON'T BE DISCOURAGED. BUT DONE LIKE DID...

Problem 1 (a) $C_L = 0.8$ pf

$C_{g(min)} = 4 \times 10^{-4}$ pf $\times (6 \times 6)\mu m^2 = .0144$ pf

$$Y = \frac{C_L}{C_g} = \frac{0.8}{0.0144} = 55.6$$

For min delay, ratio of successive sizes (f) = e.

$f^N = Y$, $N = \ln_e Y = \ln(55.6) = 4.017$

$\therefore N = 4$ stages

Grading: Calc. Err: ~ −4 ; Incorr. form ~ −8

(b) Trickier than it looks: Array contains 256 pairs of inverters.

3 SLIDES

i.e. 16 rows of 16 cells × 2 inv. per cell (4 per cell pair)

- However, only half can be on at one time Maximum.
- First of each pair is approx 5 □'s long when "on"
- Second is " 6 1/6 □'s " " "
- So worst case is when all "1st" inverters "on".
- In this case, $I_{total} = 256 \times \frac{5^V}{5 \times 10^{-4}} = 25.6$ ma
- Wires can carry max 1 ma/mm²; But are 1μm thick, so:

$\therefore$ WIRES ≥ 25.6 μm wide −3

Grading: Calc errors −3 to −4; Invalid Assump: −4 to −6; Forgot pulldown R

Problem 2: Most people did O.K. Most PLA's matched the logic equations used.

Errors were in manipulation of logic equations, or in not getting minimum # p-terms.

Grading: −4 to −6 for log. eqn error(s)
−3 for not minimizing # p terms
−3 for PLA coding error

Problem 3:

(a) Yellow implant must be 1½ λ from neighboring enh. mode transistor gate region (SLIDE)

Some said metal not over cuts, but look closely, O.K.

(b) Several Major Errors: (SLIDE)

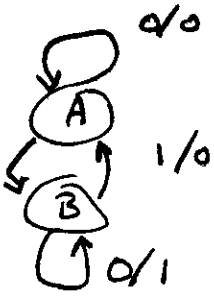
> Ratio should be 8:1, not 4:1.
> No implant over pullup to make depl. mode.
> Metal over Butting contact is 2λ not 3λ from GND METAL.
> Some DIFFS ARE 2λ sep. not 3λ.

(c) EXAMPLES OF REAL IMPROV. IN DESC. LAYOUTS OVER WHAT CIF CAN DO:

> DIG AT CORNERS OF BOXES / NOT CTR)
> DIRECT ITERATION (AS IN INFORM. DESC. LANG IN CHAP 4)
> PASS PARAMETERS TO CALLED SYMBOL: USE FOR EXAMPLE: SCALING
> USE #'S OTHER THAN JUST INTEGERS, ALLOWING EASY SPEC OF SIZES IN λ.
> CALL SYMBOLS BY NAME INST OF #.

, etc.

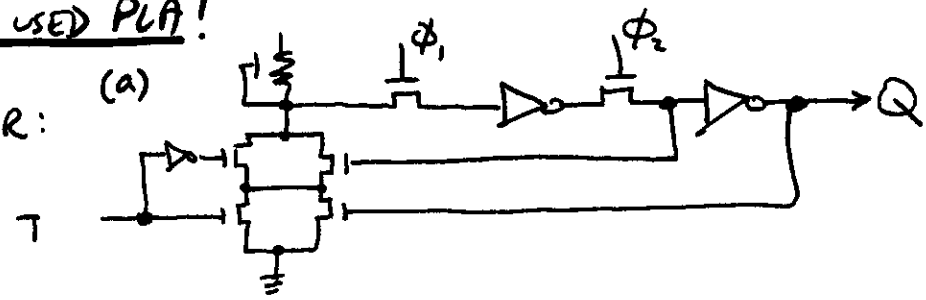
PROBLEM 4: T → TFF → Q



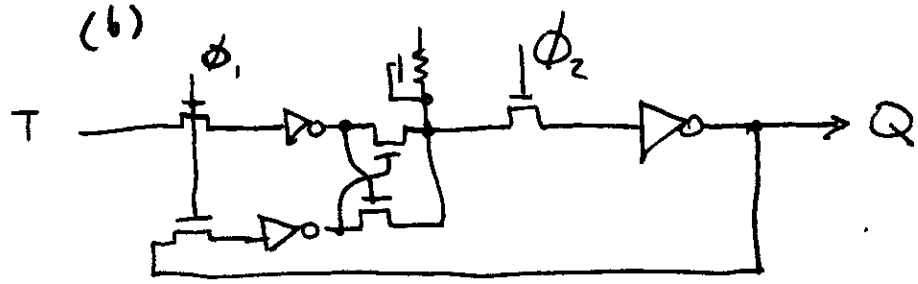
MANY SOLNS: A FEW USED PLA!

- SOME BASED ON XOR:

(a)



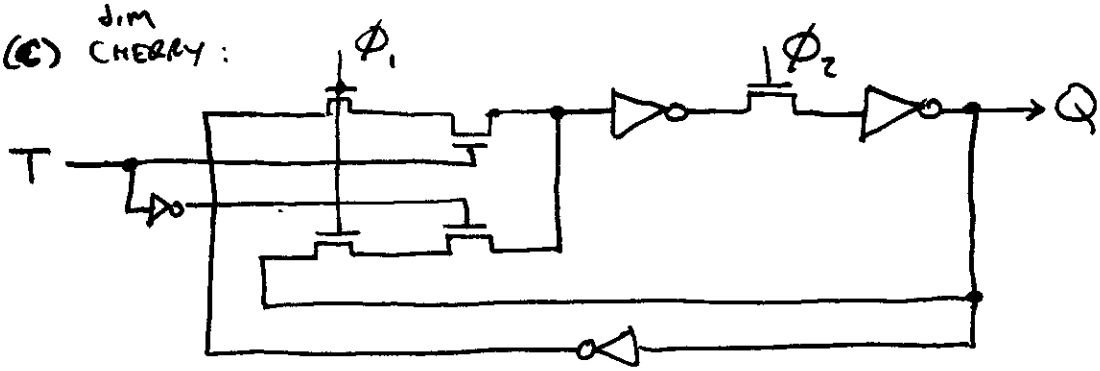
(b)



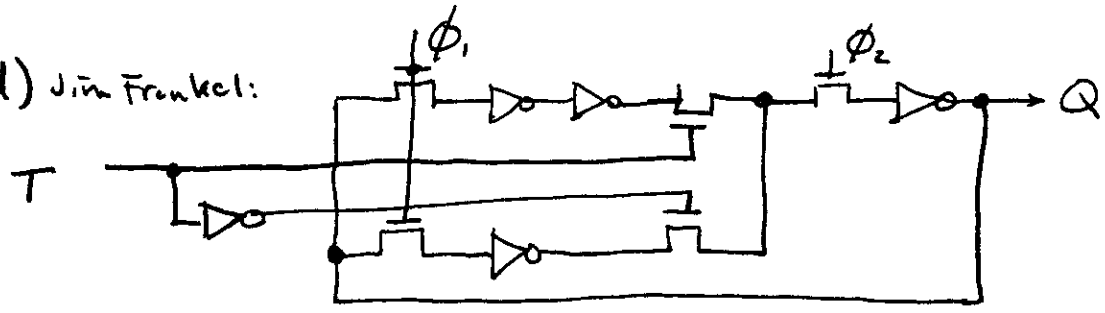
- OTHERS:

Based on Polarity Selecting inverted or non inverted feedback based on value of T

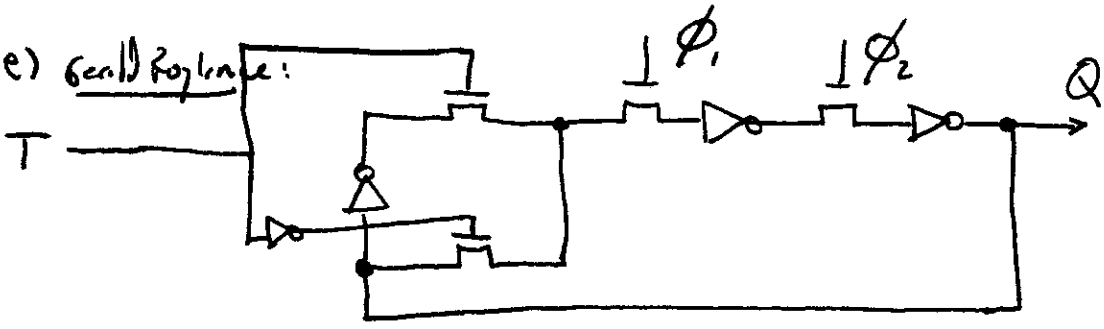
(c) Jim CHERRY:



(d) Jim Frankel:



(e) Gerald Roylance:

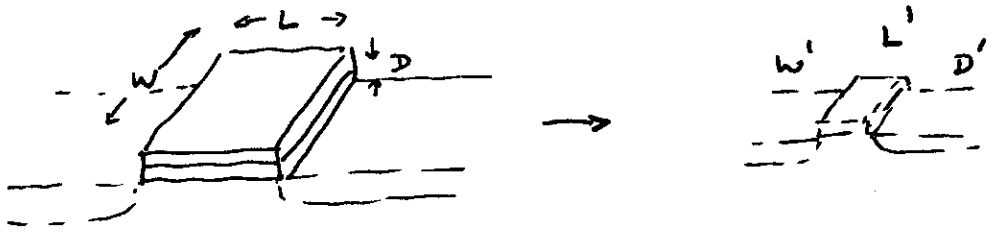


WHAT HAPPENS AS WE MAKE THINGS SMALLER?

i.e. as $\lambda \rightarrow \lambda/\alpha$ IN FUTURE

THE EFFECTS OF SCALING DOWN DIMENSIONS OF INT. SYSTEMS:

SUPPOSE WE USE A NEW PROCESS IN FUTURE, SO THAT ALL DIMENSIONS PARALLEL TO SURFACE & VERT ARE REDUCED BY A FACTOR α. WHAT WILL BE EFFECTS ON ELECTRICAL PROP OF DEVICES?



- Distances divided by α: $W' = \frac{W}{\alpha}$; $L' = \frac{L}{\alpha}$; $D' = \frac{D}{\alpha}$
- Also, to keep all Electric Fields same as before, we reduce VDD and set all thresholds to be reduced by same factor α.
- This is a particularly simple form of scaling to analyze. The actual forms used will differ as we approach extremely small device sizes, but this form may take us down to or under 1 μm feature sizes ($\lambda = 1/2\,\mu m$).
- Now what happens to τ, to C_g, to I_{ds}, etc?
- Remember Eqn 1(CH.1): $\tau = L^2/\mu V_{ds}$

$$\therefore \frac{\tau'}{\tau} = \frac{(L/\alpha)^2}{(V/\alpha)\cdot L^2/V} = \frac{1/\alpha^2}{1/\alpha} = 1/\alpha$$

$$\therefore \boxed{\tau' = \tau/\alpha}$$

Transit time of min devices, & thus circuit speeds all scale down linearly with α

- Gate Capacitance: $C_g = \epsilon WL/D$

$$\frac{C_g'}{C_g} = \frac{(L/\alpha)\cdot(W/\alpha)}{(D/\alpha)}\cdot\frac{1}{WL/D} = 1/\alpha \qquad \boxed{C_g' = \frac{C_g}{\alpha}}$$

- Note, however, that Capacitances in general scale up by α if given in terms of $C/\mu m^2$.

  Since for given absolute W & L, D gets thinner.

- Note: Resistances/$\square$ in general scale up by α

  since lines get thinner vertically. However, the R/$\square$ of transistors remains ~ same.

- Because of this, and because of other problems with POLY (if clumps of crystals too big R gets large, and this gets worse as get smaller), the ratio of POLY res to FET res may get worse as get smaller.

- FROM EQN 3: (CH.1) $I_{ds} = \frac{\mu \varepsilon W}{LD}(V_{gs}-V_{th})(V_{ds})$

  So $I_{ds} \propto WV^2/LD$

  $$\frac{I'}{I} = \frac{WV^2/\alpha^3}{LD/\alpha^2} \cdot \frac{1}{WV^2/LD} = \frac{1}{\alpha}$$

  $$\boxed{I'_{ds} = \frac{I_{ds}}{\alpha}}$$

- So, current per device goes down by $\frac{1}{\alpha}$
- However, # devices per unit area goes up by α^2
- $\therefore$ Current Density over the chip (if uniform design or repeated design sub-blocks) goes up linearly with α

  This is another problem: We may need METAL wires which are proportionally wider compared to previous designs as we scale down other features, if the wires are near the 1 ma/μm^2 current limit.

  One solution: Increase H/W of wires by α^2 as scale down. Some of this can be done, but impract. to do completely. So some wires get wider!

SCALING OF POWER DENSITY:

- **DC POWER DISSIPATION:** Per device $P_{dc} = I \cdot V$

  Since $I' = I/\alpha$, $V' = V/\alpha$, $\boxed{P'_{dc} = \frac{P_{dc}}{\alpha^2}}$ per device.

  But the number of devices increases as α^2. So, power density (average) over the chip (if regular pattern scaled) remains constant.

- **SWITCHING POWER:** The drivers which operate pass gates, charging & discharging capacitances, dissipate switching power. We can estimate this roughly ~~with dc power~~ by ~~calculating~~, estimating I, V during transients. But more directly:

  $P_{sw} \propto \frac{CV^2}{T}$; i.e., P_{sw} is the energy stored on the capacitance of a device, divided by the clock period or time between succ. charging/discharging. And, we know that $T \propto \tau$.

  Thus, $P_{sw} \propto \frac{WV^3}{DL}$, $\boxed{P'_{sw} = \frac{P_{sw}}{\alpha^2}}$ per device

  So both dc & sw power remain cont. per unit area.

  Note: the average dc power for most systems can be approximated by adding total P_{sw} to 1/2 the dc power resulting if all level restoring logic pulldowns were turned-on.

  [P_{sw} dis. in control drivers to pass gates].

- RULES OF THUMB FOR POWER DENSITIES:

While things don't get worse as we scale down, be careful:

> over areas of dimensions ≫ larger than wafer thickness (i.e. macroscopic dimensions), the following rough rules of thumb apply:

< 1 watt/cm²	no problem at all
2 watt/cm²	} somewhere in here, you begin to need special heat sinking
4 watt/cm²	}
> 8 watt/cm²	begin to need forced cooling of some kind to remove heat.

> As in all thermo problems, all depends on next higher context. One bolted chip in well heat sinked package may do well in still air at 4 w/cm², while a whole board packed full of them would need to have plumbing and be freon-cooled.

- What can I say to summarize: Be careful!

Calculate power dissipated by large projects or full chips. If > 2 watt/cm² you may get in trouble if want to use a lot of them.

> Ways out: There are often many ways to trade-off power vs time.

Remember, by using longer pullups/pullDowns we can keep same ratio in shift register, but use less power, at price of longer delays.

- LET'S CALCULATE PERHAPS A WORST CASE FROM AMONG OUR DESIGNS:

SHIFT REG IN FIG. 8b (CH4): THIS HAS WIDE PULLDOWN, SHORT PULLUP, EVEN THOUGH 8:1.

CELL AREA = $19\lambda \times 21\lambda = 57\mu m \times 63\mu m = 57\times10^{-4}cm \times 63\times10^{-4}cm$
$= 3591\times10^{-8}cm^2 = \underline{3.6\times10^{-5}cm^2}$

Power = $I \cdot V = \frac{5v}{60K\Omega} \cdot 5v = \underline{4.2\times10^{-4}\ watts}$

(ACTUALLY THE 10KΩ/□ IS FOR FAST TRACES ∴ IS OPTIMISTIC)

PWR/AREA = $\frac{4.2\times10^{-4}}{3.6\times10^{-5}} = 12 w/cm^2$. BUT IN SERIES ONLY 1/2 ON AT A TIME

$\therefore$ PWR/AREA $\approx$ 6 w/cm²

SO IF YOU FILLED A CHIP WITH THESE, YOU'D GET IN TROUBLE!

- AS AN ASIDE, ONLY ≈ 2K of ~~these~~ in pairs would fit on a ≈ 5mm × 5mm chip.
So how do we get 4K, 16K etc. memories, but stay within power limits?

> We don't use static cells for such memories. We store charge on capacitors. More next week

- Also, if want denser cells and have power problems, there are a variety of circuit tricks that can be used. Such as "clocked pullups". More next week.

IN GENERAL, WITHIN OUR DIG SYS, USING DES METH IN TEXT, WONT HAVE PROBLEMS. REGIONS OF WIRES AND PASS GATES DONT DISS. DC POWER, & COMP. FOR REGIONS OF DENSER ~~STUFF~~. LEV. REST. CELLS.

BUT IF MAKE REALLY BIG ARRAYS OF SR'S, STACK CELLS, ETC. CALCULATE PWR DENS. TO BE SAFE.

- IN ANY EVENT: SCALING DOES NOT MAKE THIS WORSE