6.978 INTRODUCTION TO VLSI SYSTEMS

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Handouts Today:

(i) Course abstract, goals, outline (preliminary), references
(ii) First half of Homework #1.

Welcome. New Course. Pleased to have such an outstanding group of students.

Cover Today:

> Administrative Details

Registration, a bit about homework and projects, exams, grading. The book we'll use. Materials you should bring to class.

> Course Overview:

An overview of integrated system architecture and design, and the topics to be covered in this course.

> Within the overview: an introduction to MOS technology and design in that technology. It is this portion of today's lecture on which the homework handed out will be based.
Administrative Details:

> Registration: I see some here (--- if so), Please get background questionnaire ---. Only those whom I've interviewed and approved may register for the course for credit. With the exception of faculty members, only those registered for credit may attend. No auditing.

> Textbook: A text will be distributed to those taking the course for credit. It is self-contained and should be sufficient --- unless you need to strengthen your background in some area or wish to explore the research literature. In either case use the references suggested in the text.

This is a limited printing of a text to be published by next summer. Copies are in very scarce supply. They are not replaceable. Don't lose your copy. The price is feedback - I'd appreciate attention to detail and notification of errors, comments, etc.

> Office Hours: TUES/THURS 3-5.

> BRING TO CLASS:

(i) Colored pencils, eraser, maybe colored felt tip pens - colors: Black, red, green, blue, yellow.

(ii) Grided scratch paper: Recommend white quad pads 1/4" sq

You'll need these for notes on some mail and occasion. Spot quizzes

> Assigned Readings: Periodically I'll indicate sections in the text you should read & study. These readings will often augment the lectures in major ways. - are a must. I encourage you to read ahead, skim, think about any sections that interest you.
HOMEWORK:

> Important part of course
> Shouldn't generally take too long. If it does, you've probably overlooked something basic.

> Some problems will require design & invention. In some cases, only a few students will find a solution to these. Don't be discouraged -- do what you can.

> Homework will be graded and must be handed in on time. Better to hand in partially completed HW than to wait.

> Will be assigned weekly. Sometimes handed out in parts (e.g., Tuesday). Always due following Tuesday. If you have a problem with an assignment, hand in on Tuesday, then see me during office hours that week to discuss it.

PROJECTS: I believe strongly in learning by doing, so:

> Important part of course. Will count heavily in grade.
> Will be done in stages, with various things turned in as we proceed, to make sure you'll be able to finish on time.
> Intent: Not too ambitious. Completion of a simple correct design better than an ambitious project that is incomplete or full of errors.

GRADES: During course a numerical score will be accumulated; the maximum score will be (and breakdown is):

$\text{Spot Quiz + HW (10 x 10) + MT + Final + Prelim Proj + Proj Final Report. (50) + 100 + 100 + 100 + 100 = 500 (4)}$

I'll rank students according to this score. Estimated grade boundaries by my judgement, and move a few students up/down according to my judgement of other non-score factors ---

> Questions?
Overview:

This course is about the *arch & design* of VLSI Systems.

Integration: Informally, system implemented as an integrated whole onto a monolithic material.

Show OM slide Show OM chip

Architecture vs Design vs Implementation: Printing Analogy.

In particular, A & Des. of large digital systems such as digital computers, spec. pur. syst. for signal processing, arrays of simple processors for performing matrix computations or image processing functions, etc.

VLSI: why "Very ---"? Improvements in implementation technologies have resulted in suff. circuit density so that ~ tens of thousands of transistors can be fabricated on a single chip.

It is clear that at least an order of magnitude reduction can still be made before ---. Thus, density increase of x100 or more can still be and will be made.

Individual phot ~ 4 to 6 \( \mu \text{m} \) wide, separated by 4 to 6 \( \mu \text{m} \). A micron is 1/1000 mm. Chips are ~2 to 6 mm on a side. In future, sizes can be reduced to less than 0.5 \( \mu \text{m} \).

Those interested in techniques for high-resolution litho might check out Prof. Hank Smith's course, 6.969 (Submicron Structures Technology).

The design of structures to be implemented on a chip is now an architect's game. This trend will increase in the future.
All such are composed of **finite state machines** controlling **REG-REG** data transfer path.

Thus we need only 2 basic types of building blocks: **registers** and **combinational logic (C/L)**

**Sketch**

**Example**: stored program computer:

```
<table>
<thead>
<tr>
<th>Finite State Machine</th>
</tr>
</thead>
<tbody>
<tr>
<td>↑↑ ↓↓</td>
</tr>
<tr>
<td>I/O ←→ Data Path ←→ Memory</td>
</tr>
</tbody>
</table>
```

**Where**: Data path is:

```
R ↔ C/L R ↔ C/L
```

**Where**: FSM is:

```
φ₁
R → C/L → R
```

```
φ₂
R ↔ C/L ↔ R
```
We will use one very common integrated system technology in this course: **NMOS**.

The **NMOS process** fabricates systems which contain a particular type of transistor - the **Field Effect Transistor**.

Most of you will have studied junction transistors, and perhaps bipolar integrated circuit technology.

**MOS-FETs** are much simpler in concept, structure, and in their topological properties. You should not try to correlate their properties with junction transistors. Treat them as a new sort of entity.

**Registers**, **combinational logic**, and their interconnections are very easy to design and implement in **NMOS**.

The challenge will be to take advantage of this, to think up architectures, to design large digital structures in a reasonably systematic way, so as to contain their complexity, to describe these structures formally, and to implement them quickly.

The course will develop a particular design methodology for systematically designing large digital systems in **NMOS**.

The methodology will apply rules & constraints to the successive mappings of a design as we proceed top-down from system to subsystem to logic to circuit to **strikethrough** (topology) design to layout levels of design.

I'll place great emphasis on visualizing & manipulating multiple levels of representation, returning to any one level.
Now, let's look at NMOS in more detail, before continuing overview. Homework #1: Based on this.

I'd like to develop the basic ideas of how systems are integrated in NMOS technology.

Visualize a chip as being a sort of 3-level printed circuit board. 3-levels of conducting material are sandwiched between insulating material. Show VG sequence.

By photolithography we can pattern the conducting material to make contact cuts thru the insulating material to form "wires" on the various levels. Show V6 sequence.

Color codes/level names

White screens on levels may cross with no functional effect, except where RED crosses Green a transistor is created, which has the properties of a simple switch:

```
\[ \text{layout} \quad \rightarrow \quad \text{circuit symbol} \quad \rightarrow \quad \text{function} \]
```

What could we do with these? Let's look at some simple examples of digital functions we can very easily implement using simple groups of switches, wired together in particular ways.

Will use a color-coded "stick diagram" to describe these structures.
EX NMOS C/L FUNCTIONS: TOPOLOGY

EXAMPLE: const. stick dia. of MOS integrated structure to implement a 4 to 1 selector:

\[
\begin{array}{c|c|c|c}
\text{A} & \text{B} & \text{Z} \\
\hline
0 & 0 & S_0 \\
0 & 1 & S_1 \\
1 & 0 & S_2 \\
1 & 1 & S_3 \\
\end{array}
\]

SOLUTION:

CORRECT TRANSISOR DIAGRAM:

CIRCUIT

Interestingly, we will often find it easier & more optimal to design in this way (reminiscent of early relay switching logic) rather than use the formal methods of design synthesis using logic gates such by switching.
EXAMPLE: Construct stick diagram of MOS integrated structure to implement a tally function of 3 inputs:

- N input variables, N+1 outputs.
- If M input are eq 1, output # M = 1

<table>
<thead>
<tr>
<th>X1, X2, X3</th>
<th>Z0</th>
<th>Z1</th>
<th>Z2</th>
<th>Z3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>0 0 0 1 0 0 0 0</td>
<td></td>
<td></td>
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<td>0 0 1</td>
<td>0 0 1 0 1 0 0 0</td>
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</table>

A SOLUTION:
We'll study enough about the electrical properties of the MOS Transistor and simple circuits composed of these, so that we can:

(i) Flesh out our stick diagrams to form the geometric layouts of Transistors and wires of correct size to implement working circuits.

(ii) To be able to predict the performance of circuits in our systems: i.e. signal propagation delays and power consumption.

We will study enough about the patterning & fabrication technologies used in industry to:

(i) Develop a set of Design Rules which place additional constraints on the geometries of our layouts, i.e. on how narrow line-widths can be, and on how small the line separations can be.

(ii) Develop a symbolic language for formally specifying our layout geometries, so our designs can be input to industrial pattern generation machines which make the starting patterns to make masks.

(iii) Understand the patterning & masking & fab information needed to go along with designs, so we can really get designs implemented by commercial firms.

Slides on PG - Mask - Chip

Show artifacts
PROJECTS

I believe the best way to learn and master this material is by actually doing it - from top to bottom.

So, we will each do a project. Nothing too ambitious, but enough to be able to visualize every step from architecture to finished chip. More...

MULTI-PROJECT CHIP IDEA

SHOW SLIDE

FOR A SOURCE OF EXAMPLE SUBSYSTEMS & CIRCUIT LAYOUTS, FOR VISUALIZATION OF A COMPLETE SYSTEM. DES. USING THE METHODOLOGY OF THE COURSE, WE'LL ANALYZE THE CALTECH "OM" COMPUTER IN SOME DETAIL.

NOW WE'LL BE PREPARED TO LOOK AHEAD. THE DESIGN & PROJECT EXPERIENCE WILL GIVE US THE CONTEXT TO DISCUSS THE FUTURE OF INTEGRATED SYSTEM ARCHITECTURE & TECHNOLOGY, AND TO SEE WHERE THE OPEN QUESTIONS ARE, WHERE THE RESEARCH OPPORTUNITIES ARE:

SOME TOPICS:

(i) SCALING & PHYSICAL LIMITS
(ii) DESIGN METHODOLOGY
(iii) SYSTEMS TO AID/ENHANCE DESIGN
(iv) SYSTEM TIMING & SYNCHRONIZATION
(v) ARCHITECTURE FOR CONCURRENT PROCESSING
(vi) PHYSICS OF COMPUTATIONAL SYSTEMS

HOPING THAT CARL VAN MEAD WILL BE ABLE TO VISIT FOR A FEW DAYS LATE IN THE COURSE & GIVE SEVERAL LECTURES ON THESE TOPICS.

QUESTIONS?