LECT 1, 12 SEP

6.978 INTRODUCTION TO VLSI SYSTEMS

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Handouts Today:

(i) Course abstract, goals, outline (preliminary), references
(ii) First half of Homework #1.

Cover Today:

Welcome. New Course. Pleased to have such an outstanding group of students.

> Administrative Details

Registration, a bit about homework and projects, exams, grading. The book we'll use. Materials you should bring to class

> Course Overview:

An overview of integrated system architecture and design, and the topics to be covered in this course.

> Within the Overview: an introduction to MOS technology and design in that technology. It is this portion of todays lecture on which the Homework handed out will be based.

Administrative Details:

> **Registration:** I see some here (--- if so). Please get background questionnaire ---.

Only those whom I've interviewed and approved may register for the course for credit.

With the exception of Faculty members, only those registered for credit may attend. No auditing.

> **Textbook:** A text will be distributed to those taking the course for credit. It is self contained and should be sufficient --- unless you need to strengthen your background in some area or wish to explore the research literature. In either case use the references suggested in the text.

This is a limited printing of a text to be published by next summer. Copies are in very scarce supply. They are not replaceable. Don't lose your copy. The price is feedback - I'd appreciate attention to detail and notification of errors, comments, etc.

> **OFFICE HOURS:** TUES/THURS 3-5.
> WED 10-4 (STARTING NEXT WEEK)

> **BRING TO CLASS:**

(i) COLORED PENCILS, ERASER, MAYBE COLORED FELT TIP PENS.
COLORS: BLACK, RED, GREEN, BLUE, YELLOW.

(ii) GRIDDED SCRATCH PAPER: RECOMMEND WHITE QUAD. PADS 1/4" SQ

YOU'LL NEED THESE FOR NOTES ON SOME MATL & OCCAS. SPOT QUIZZES

> **ASSIGNED READINGS:** Periodically I'll indicate sections in the text you should read & study. Those readings will often augment the lectures in major ways - are a must. I encourage you to read ahead, skim, think about any sections that interest you

HOMEWORK:

> IMPORTANT PART OF COURSE

> SHOULDN'T GENERALLY TAKE TOO LONG. IF IT DOES, YOU'VE PROBABLY OVERLOOKED SOMETHING BASIC.

> SOME PROBLEMS WILL REQUIRE DESIGN & INVENTION. IN SOME CASES ONLY A FEW STUDENTS WILL FIND A SOLUTION TO THESE. DON'T BE DISCOURAGED --- DO WHAT YOU CAN.

> HOMEWORK WILL BE GRADED AND MUST BE HANDED-IN ON TIME. BETTER TO HAND IN PARTIALLY COMPLETED HW THAN TO WAIT.

> WILL BE ASSIGNED WEEKLY. SOMETIMES HANDED OUT IN PARTS (TUE --- THUR). ALWAYS DUE FOLLOWING TUESDAY. IF YOU HAVE A PROBLEM WITH AN ASSIGNMENT, HAND IN ON TIME, THEN SEE ME DURING OFFICE HOURS THAT WEEK TO DISCUSS IT.

PROJECTS: I believe strongly in learning by doing, so:

> IMPORTANT PART OF COURSE. WILL COUNT HEAVILY IN GRADE.

> WILL BE DONE IN STAGES, WITH VARIOUS THINGS TURNED IN AS WE PROCEED, TO MAKE SURE YOU'LL BE ABLE TO FINISH ON TIME.

> INTENT: NOT TOO AMBITIOUS. COMPLETION OF A SIMPLE CORRECT DESIGN MUCH BETTER THAN AN AMBITIOUS PROJECT THAT IS INCOMPLETE OR FULL OF ERRORS.

GRADES: During course a numerical score will be accumulated: The maximum score will be (and breakdown is):

SPOT QUIZES	+ HW (10 x 10)	+ MT	+ FINAL	+ PRELIM PROJ	+ PROJ FINAL REPORT.
(50)	+ 100	+ 100	+ 100	+ 100	+ 100 = 500(+)

I'll RANK STUDENTS ACC. TO THIS SCORE. EST. GRADE BOUNDARIES BY MY JUDGEMENT, AND MOVE A FEW STUDENTS UP/DOWN ACCORDING TO MY JUDGEMENT OF OTHER NON-SCORE FACTORS ---

> QUESTIONS?

Overview:

> This course is about the arch & design of VLSI systems

Integ. System: Informally, system implemented as an integrated whole onto a monolithic material.

Show OM slide Show OM chip

Architecture & Design vs Implementation: Printing Analogy.

> In Particular, A & Des. of large digital systems such as digital computers, spec. pur. syst. for signal processing, arrays of simple processors for performing matrix computations of image processing functions, etc.

> VLSI: why "Very---"? Improvements in Implementation technologies have resulted in Suff. circuit density so that ~ tens of thousands of transistors can be fabricated on a single chip.

It is clear that at least an order of mag linear reduction can still be ~~made before~~. Thus, density increase of ~~x~~100 or more can still be and will be made.

BLACKBOARD

Individual paths ~ 4 to 6 μ wide, ~~separated by~~ 4 to 6 μ. A micron is 1/1000 mm. Chips are ~2 to 6 mm on a side. In future, lines can be reduced to less than 0.5 μ.

Those interested in techniques for high-resolution lithog might check out Prof. Hank Smith's course, 6.969 (Submicron Structures Technology)

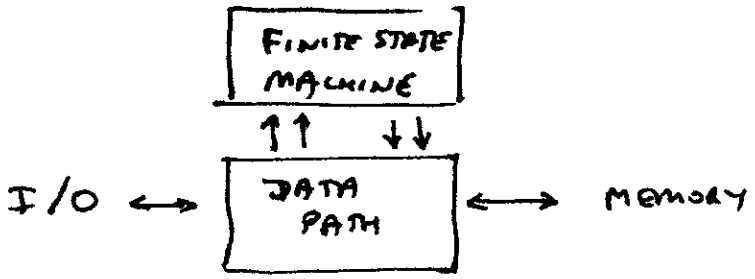
The Design of structures to be implemented on a chip is now an architects game. This trend will increase in the future.

> So, Arch & Des of (Synchr.) Dig. Systems.

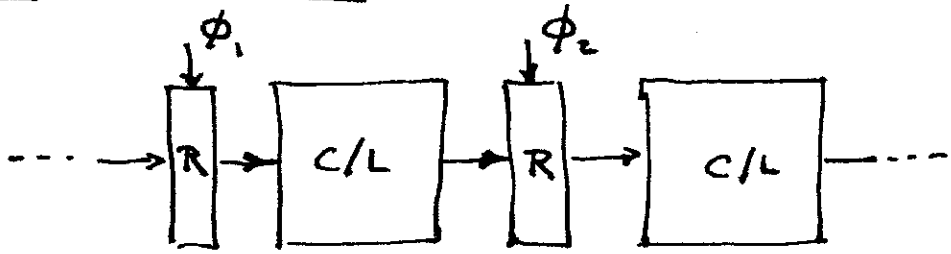
All such are composed of FINITE STATE MACHINES CONTROLLING REG-REG DATA TRANSFER PATHS

Thus we need only 2 basic types of building blocks: REGISTERS & COMBINATIONAL LOGIC (C/L)

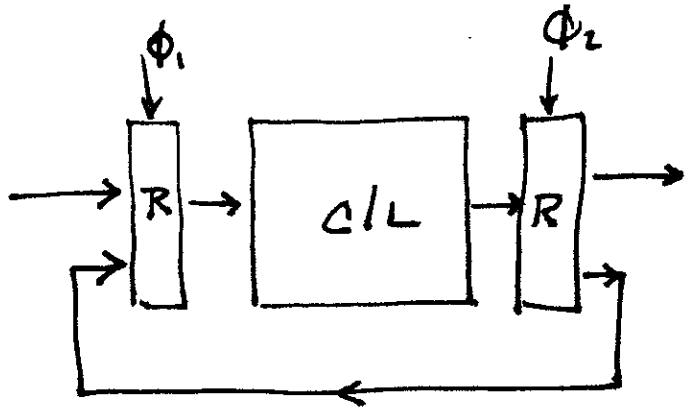
Sketch on Board } EXAMPLE: STORED PROGRAM COMPUTER:



WHERE: DATA PATH IS:



& WHERE FSM IS:



> We will use one very common integrated system technology in this course: nMOS.

The nMOS process fabricates systems which contain a particular type of transistor - the Field Effect Transistor.

Most of you will have studied junction transistors, and perhaps bipolar integrated circuit technology.

MOS-FETs are much simpler in concept, structure, and in their topological properties. You should not try to correlate their properties with junction transistor. Treat them as a new sort of entity.

> REGISTERS, COMBINATIONAL LOGIC, AND their interconnections are very easy to design & implement in nMOS.

> The challenge will be to take advantage of this, to think up architectures, to design large digital structures in a reasonably systematic way, so as to contain their complexity, to describe these structures formally, and to implement them quickly.

> The course will develop a particular design methodology for systematically designing large digital systems in nMOS.

> The methodology will apply rules & constraints to the successive mappings of a design as we proceed top-down from system to subsystem to logic to circuit to stick (topology) diagram to layout levels of design.

> I'll place great emphasis on visualizing & manipulating multiple levels of representation, rather than pushing for expertise at any one level.

NOW, LETS LOOK AT nMOS in MORE DETAIL, BEFORE CONTINUING OVERVIEW. HOMEWORK #1 BASED ON THIS

NMOS 1

> I'd like to develop the basic ideas of how systems are integrated in nMOS technology.

FLIP SCREEN

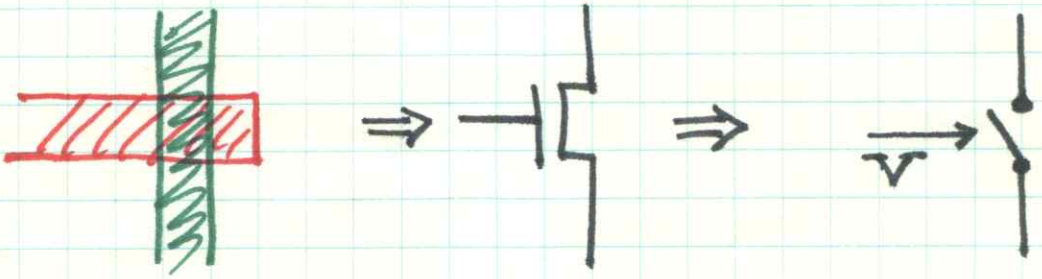
USE WHITE BOARD

VISUALIZE a chip as being a sort of 3-level printed circuit board. 3-levels of conducting material are sandwiched between insulating material. SHOW VG Sequence. Names

By photolithography we can pattern the conducting material & make contact cuts thru the insulating material to form "WIRES" on the various levels. SHOW V6 Sequence

Color codes / Level Names

> Wires on levels may cross with no functional effect, except, where RED crosses Green a transistor is created, which has the properties of a simple switch:



layout circuit symbol "function"

C/L

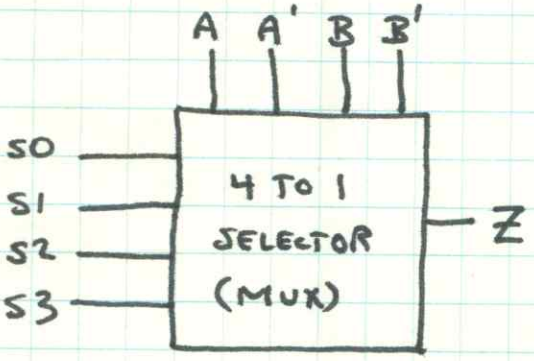
> WHAT COULD WE DO WITH THESE? Lets look at some simple examples of digital functions we can very easily implement using simple groups of switches, wired together in particular ways.

S/L

> WILL USE A COLOR-CODED "STICK DIAGRAM" TO DESCRIBE THESE STRUCTURES.

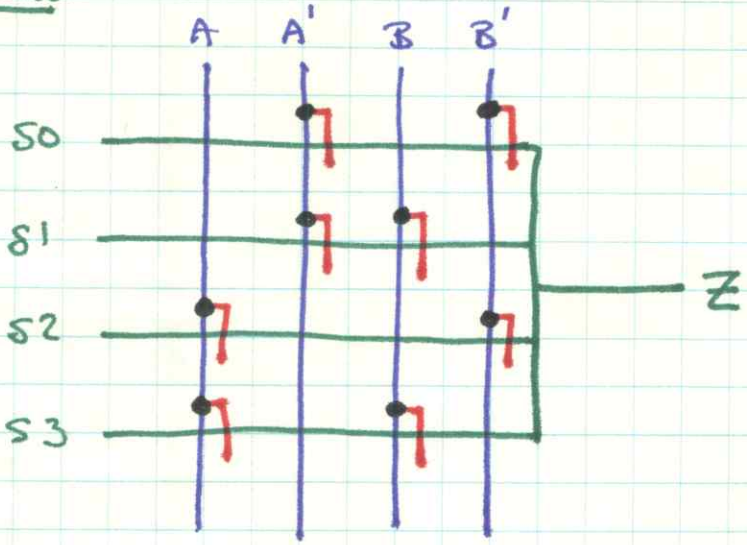
EX nMOS C/L FUNCTIONS: TOPOLOGY

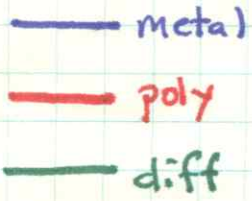
EXAMPLE: CONST. STICK DIAG OF MOS INTEGRATED STRUCTURE TO IMPLEMENT A 4 TO 1 SELECTOR:



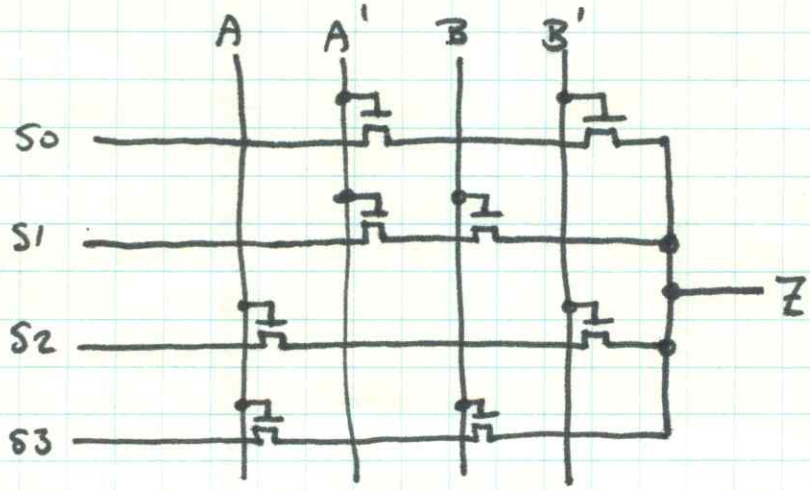
A	B	Z
0	0	S0
0	1	S1
1	0	S2
1	1	S3

SOLUTION:





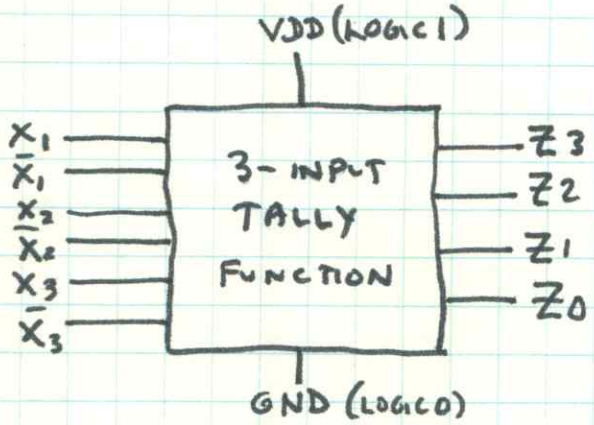
CORRES. TRANSISTOR DIAGRAM: CIRCUIT



> Interestingly, we will often find it easier & more optimal to design in this way (reminiscent of early relay switching logic) rather than use the formal methods of design synthesis using logic gates given by switching fns

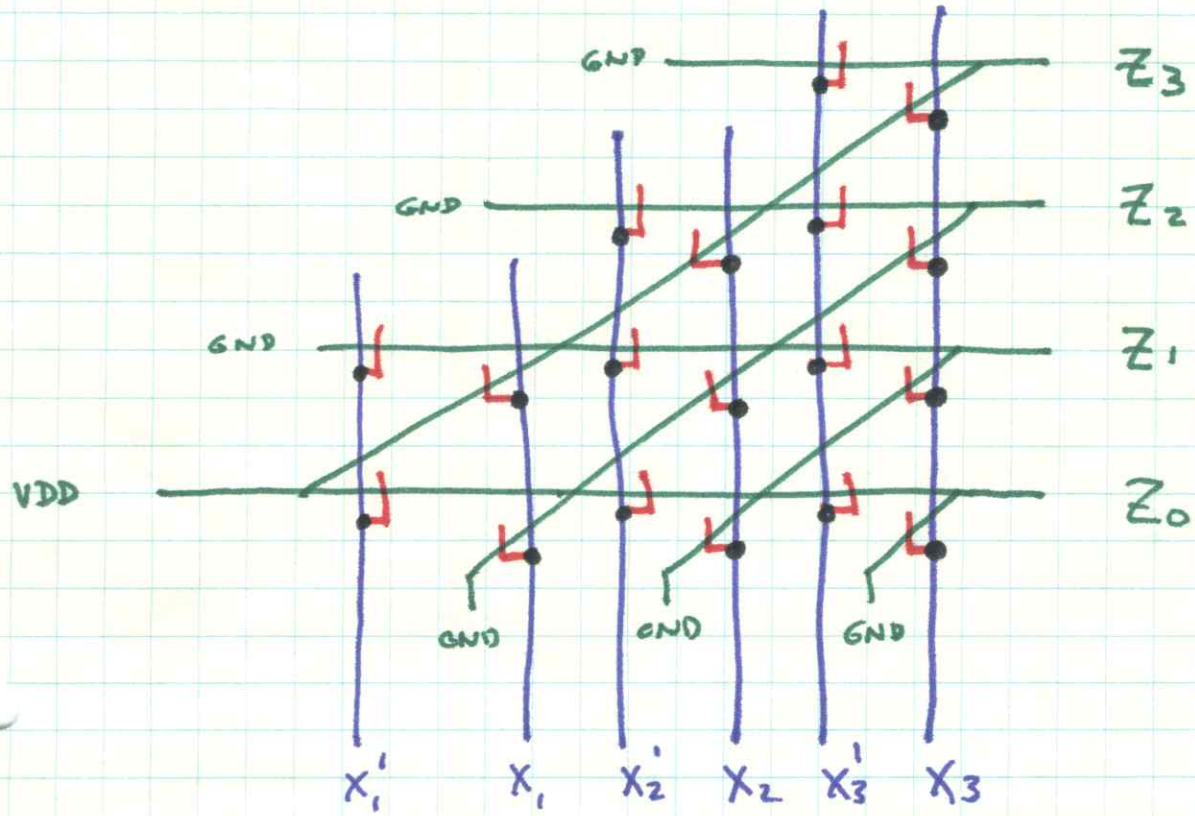
EXAMPLE: CONST. STICK DIAGRAM OF MOS INTEGRATED STRUCTURE TO IMPLEMENT A TALLY FUNCTION OF 3 INPUTS:

N INPUT VARIABLES, N+1 OUTPUTS.
IF M INPUT ARE EQ 1, OUTPUT # M = 1



X_1	X_2	X_3	Z_0	Z_1	Z_2	Z_3
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	1	0	0
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	0	1	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

A SOLUTION:



OVERVIEW (CONT.)

> We'll study enough about the electrical properties of the MOS Transistor and simple circuits composed of these, so that we can:

(i) flesh out our stick diagrams to form the geometric layouts of Transistors and wires of correct size to implement working circuits.

(ii) & to be able to predict the performance of circuits in our systems: i.e. signal propogation delays and power consumption.

> We will study enough about the patterning & fabrication technologies used in industry to:

(i) develop a set of Design Rules which place additional constraints on the geometrics of our layouts, i.e. on how narrow line-widths can be [illegible] on how small the line separations can be DES. RULE SLIDE

(ii) develop a symbolic language for formally

Specifying our layout geometries, so our designs can be input to Industrial Pattern Generation machines which make the starting patterns to make masks

(iii) understand the patterning & masking & fab information needed to go along with designs so we can really get designs implemented by commercial firms.

SLIDES ON PG - MASK - CHIP

SHOW ARTIFACTS

> PROJECTS

I believe the best way to learn and master this material is by actually doing it - from top to bottom.

So, we will each do a project. Nothing real ambitious, but enough to be able to visualize every step from architecture to finished chip. More ---

> MULTI-PROJECT CHIP IDEA **SHOW SLIDE**

> FOR A SOURCE OF EXAMPLE SUBSYSTEMS & CIRCUIT LAYOUTS, FOR VISUALIZATION OF A COMPLETE SYSTEM DES. USING THE METHODOLOGY OF THE COURSE, WE'LL ANALYZE THE CALTECH "OM" COMPUTERS IN SOME DETAIL.

> NOW WE'LL BE PREPARED TO LOOK AHEAD. THE DESIGN & PROJECT EXPERIENCE WILL GIVE US THE CONTEXT TO DISCUSS THE FUTURE OF INTEGRATED SYSTEM ARCHITECTURE & TECHNOLOGY, AND TO SEE WHAT THE OPEN QUESTIONS ARE, WHERE THE RESEARCH OPPORTUNITIES ARE:

SOME TOPICS:

(i) SCALING & PHYSICAL LIMITS
(ii) DESIGN METHODOLOGY
(iii) SYSTEMS TO AID/ENHANCE DESIGN
(iv) SYSTEM TIMING & SYNCHRONIZATION
(v) ARCHITECTURE FOR CONCURRENT PROCESSING
(vi) PHYSICS OF COMPUTATIONAL SYSTEMS

HOPING THAT CARVER MEAD WILL BE ABLE TO VISIT FOR A FEW DAYS LATE IN THE COURSE & GIVE SEVERAL LECTURES ON THESE TOPICS.

> QUESTIONS?