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Basic Limitations in Microcircuit Fabrication Technology

Ivan E. Sutherland, Carver A. Mead, and Thomas E. Everhart

A Report prepared for

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY

Rand
SANTA MONICA, CA. 90406

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PREFACE

This report presents the findings of a 6-month study undertaken for the Defense Advanced Research Projects Agency to ascertain what, if any, research ARPA might sensibly conduct in integrated microcircuit technology. The authors entered upon the study through a conviction that serious international competition in this technology may appear in the next few years, and a desire to ensure for the United States as favorable an opportunity to meet this competition as research can make available. Both the ubiquitous nature of micro-electronics in defense applications and the particularly severe special defense requirements for complex, low-power, micro-miniaturized circuitry make a commanding lead in this technology very important. The authors wished to assure themselves and ARPA that the existing research programs provide adequately for the forthcoming needs of the nation. The report details some high-leverage research areas, not now receiving government or private support, where relatively small, advanced research efforts may have substantial payoff. No endorsement of the study conclusions by ARPA is implied or intended.

During the course of the study, the authors visited major laboratories having a capability for making very small circuitry. In nearly every visit, discussions with the research personnel were complete and frank. The authors believe that they have seen all the major U.S. activities aimed at producing circuits of submicron dimensions.

It was quickly realized that U.S. industry is treating the new developments in microcircuit technology as a continuation of the coupled evolution of decreasing size of circuit features and increasing complexity of logical units that has been so effective in the past. The authors therefore asked each industrial group specific questions about its aspirations for very-small-size circuits of modest complexity. The responses were disappointingly conservative. There is such a wide variety of problems to be overcome in developing a submicron circuit technology, and those experienced in the field have seen so many "rocks in the road," that relatively slow progress is the most that they can

foresee. Moreover, the only developments economically justifiable for private support must maintain as high a level of complexity as possible. The authors, as a group, believe that a more direct push toward very small circuitry, albeit of modest complexity, will pay off handsomely.

The three authors of this report bring a wide range of experience to bear on the study. Carver Mead, Professor of Electrical Engineering at the California Institute of Technology, is an expert in semiconductor physics; he has contributed importantly to an understanding of the fundamental physical principles that limit how small semiconductor circuitry can be made. Thomas Everhart, Chairman of the Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley, is an expert in electron microscopy; he was one of the earliest builders of fine-resolution electron beam systems. Ivan Sutherland, a member of the Rand staff when this report was prepared and now Professor of Computer Science, California Institute of Technology, is an expert in systems design; he has done much fundamental work in large systems for computer graphics. Together they have sought to understand what limitations to microcircuit fabrication are fundamental. They have tried to "orthogonalize" the tasks in order to determine separate areas where progress can be made, identifying those areas adequately covered by existing development programs and highlighting those where relatively little work is being done.

The potential for future capability revealed by this study is truly impressive. There is every reason to believe that the integrated circuit revolution has run only half its course; the change in complexity of four to five orders of magnitude that has taken place during the past 15 years appears to be only the first half of a potential eight-order-of-magnitude development. There seem to be no fundamental obstacles to 10^7 to 10^8 device integrated circuits. The authors hope that their efforts may contribute to having such circuits sooner than would otherwise be the case.

Finally, the authors are indebted to the foresights of Rand's sponsors in ARPA, to the cooperation of the many technical experts in industry who gave so generously of their time and knowledge, and to the many people at Rand and at Science Applications, Inc. without whose help their efforts would not have borne fruit.

SUMMARY AND RECOMMENDATIONS

Today's microcircuit fabrication industry is operating against two fundamental limits: the wavelength of visible light and the number of elements that can be reproduced with a single alignment. The use of electron beams, ultraviolet light, and X-rays makes fabrication of submicron geometry devices possible. On the other hand, because no significant improvements in the number of devices reproduced per alignment are anticipated, substantial changes in the patterning processes are likely.

In spite of the revolutionary nature of the changes in fabrication and design methods imposed by submicron geometries, U.S. industry appears to be treating these changes as further incremental progress. There seems to be little evidence of work aimed at quickly reaching the fundamental limits to device size imposed by physical theory. More effort needs to be devoted to improving the organization of circuitry to provide the most computation per unit area of circuit. Unless positive steps are taken, the existing U.S. investment in today's fabrication methods may be made obsolete by the new fabrication technologies, producing less vigorous competition domestically, and placing the United States in a disadvantageous position in defense and international trade.

Although at first glance it appears that the microcircuit fabrication technology has adequate funding from private sources and ample economic justification to ensure continued private funding, the existing research efforts are aimed at a continuing gradual decrease in feature size and a corresponding gradual increase in performance, coupled tightly to ever-increasing complexity levels. The following four important activities, not now covered by private funds, should be considered for future funding:

(1) *Efforts aimed at making very small devices.* Such efforts would set aside for the time being the push toward more complicated devices and focus instead on making quite simple circuits with the smallest possible feature sizes. Such efforts would not only serve to verify the limits to transistor size predicted theoretically, but also

serve as a test bed for the fabrication and electronic design techniques required for these small dimensions.

(2) *Efforts aimed at measuring the limits of dimensional stability of silicon substrates and mask materials.* Such efforts would require very precise dimensional measurements over silicon wafers and mask materials before and after various processing steps. If the values of anomalous dimensional distortions were known, they would serve as an important input to the designers of replication processes. If processing steps that minimize distortions can be identified, they might form the basis of further improvements in replication precision.

(3) *Efforts aimed at predicting the optimum feature size, die size, and wafer size, given the constraints of the newly evolving technology.* It is apparent that the fundamental limits to pattern replication precision provided by the dimensional stability of silicon have been or soon will be reached. Further decrease in feature size will require multiple replication steps on each wafer, thus making wafer size independent of the pattern replication steps and presenting new freedoms and new difficulties in the manufacturing processes. The trend toward larger wafers has been driven by a desire to reduce the unit cost of handling, as has the drive to maintain a single alignment step per wafer. In a technology that can no longer satisfy both of these requirements, what is the most effective compromise to make? To what extent is this choice dictated by our existing capital investment in large wafers? If one were starting anew, as our international competitors are, what choices would one prefer to make?

(4) *Efforts aimed at understanding the system design implications of very-large-scale integrated circuits.* Indications are that great benefits may be obtained by improving the arrangement of memory and processing power implemented in the more complex circuits that will be available in the near future. Questions that need to be answered are: How should computations be organized so as to obtain maximum performance with minimum silicon area? What advantages can be gained by making "smart" memories that can compute as well as store? How can complex machines be configured to minimize the software burden on their users? How are organizations of 10^5 or 10^6 gates different in kind from today's

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