Reminiscences of the VLSI Revolution: A Timeline of Events

By Lynn Conway

Date	Timeline Sections and Lists of Events
	Lynn Conway's early career:
Jun 64	Conway is recruited by IBM Research
Spring 65	Joins the IBM-ACS supercomputer project
1965-68	Works on multi-level simulation of ACS-1
Sep 65	Invents multiple--issue dynamic instruction scheduling (DIS), a foundational paradigm of ACS-1's architecture
Aug 6, 68	Proposes a design of the multiple-level-of-abstraction ACS computer-design-process
Aug 29, 68	Conway is fired after informing IBM of her plans for gender transition
Spring 69	Completes her gender transition, and quietly restarts her career in 'stealth mode,' in a new identity
Oct 13, 69	Conway joins Memorex
Mid 71	Becomes CPU architect of MRX 30 computer system
Fall 72	Memorex leaves computer business
Oct 8, 73	Conway joins Xerox PARC, as architect/designer of the Sierra compound OCR/FAX system
Fall 75	Bert Sutherland, Lynn's new lab manager, cancels the Sierra Project
	Early events in Large Scale Integration (LSI):
Apr 19, 65	Gordon Moore postulates LSI scaling effects
66	Robert Bower, et al, invent self-aligned gate MOS fabrication technology
66-68	Frank Wanlass, Bob Booher and Lee Boysel innovate and evolve MOS dynamic-logic circuit-design methods
Apr 70	Lee Boysel publishes MOS circuit design methods innovated at Fairchild and Four-Phase Systems
70	Carver Mead coins the term "Moore's Law"
70	Federico Faggin advances Intel's MOS circuit design methods
Nov 15, 71	Intel introduces the 4004 microprocessor, which uses the emerging MOS circuit-design methods
71	Mead begins teaching MOS circuit design at Caltech
72	Bruce Hoenisen & Mead calculate the physical limits of MOS scaling
Oct 74	Robert Dennard calculates the effects of MOS scaling on system performance
late(?) 74	Ivan Sutherland becomes chair of Computer Science at Caltech; recuits Mead to the new department
75	Sutherland, Mead & Tom Everhart conduct ARPA study of basic limits of microelectronic fabrication technology

Xerox PARC/Caltech collaborate to explore chip-design complexity problem:

Fall 75	Early meetings, discussions and brainstorming begins at PARC and Caltech
Jan 26, 76	Ivan Sutherland proposes formal PARC/Caltech collaboration in a letter to Bert Sutherland
76	Conway, Fairbairn (PARC) and Mead, Rowson, Johannsen (Caltech) begin an intensive research collaboration
76	Doug Fairbairn and Jim Rowson protoype ICARUS interactive graphical chip layout system
76	Ivan Sutherland and Ron Ayres at Caltech create CIF1.0 graphical interchange format for layout specs
76	Caltech: Mike Tolle, Ivan Sutherland, et al, design "OM" data path chip, using Ron Ayres ICL/ICLIC symbolic layout software
Fall 76	Sutherland and Mead begin writing Scientific American article (publ Nov 77) on open challenges faced as 76 came to a close.
Nov 76	ARPA publishes the '75 study by Sutherland, Mead & Everhart on basic limits of fabrication technology

Shifting the paradigm: creating new VLSI system design methods:

Late 76	Conway senses Steinmetz analogy: need for restructuring, simplification, codification of entire space of chip design abstractions.
Early 77	Conway proposes that she and Mead craft a streamlined methodology for design of systems, rather than just circuits.
Spring 77	In burst of creativity, Mead and Conway coalesce a design-methodology that covers abstraction-levels from systems to silicon.
Spring 77	Conway invents λ-based scalable design rules, cracking major roadblock to effective MOS EDA
Spring 77	Fairbairn and Rowson adapt ICARUS layout system to λ-based scalable design rules
Spring 77	Conway begins to compile tutorial overview of the new methods from new paradigm point-of-view.
Jun 77	Dave Johannsen begins design of "OM2" - creating many classic subsystem design-examples under the new methods
Jun 77	Conway wonders "What to do?" with the new methods; they're too avant-garde for publication in traditional journals.

Creating and rapidly evolving a textbook to teach and validate the methods:

Jun 77	Conway proposes idea of evolving a comprehensive textbook, writing/self-publishing it using PARC's computers/printers
Jul-Aug 77	Conway launches crash effort to architect/write the text.
Oct 77	Chapters 1-3 of pre-publication draft readied for Carlo Sequin at UCB and Mead at Caltech, who provide feedback on usage
Dec 77	Johannsen completes design of OM2; Lyon, Sproull and Sequin formally define CIF2.0.
Jan 78	Overview of ICARUS and CIF2.0 descriptions readied for Chapter 4, OM2 design-examples readied for Chapter 5, of evolving text.
Feb 78	Chapters 1-5 readied for courses by Bob Sproull at CMU, Ivan Sutherland at Caltech and Fred Rosenberger at Washington Univ.

The MIT '78 VLSI System Design Course:

Early 78	Bert Sutherland urges Conway to create and teach a new form of VLSI system design course at MIT.; she accepts the challenge.
May 78	While designing the course, Conway gets idea of including QTA mask/fab of student design projects
May-Jul 78	Conway evolves course-plan, drafts course handouts; lectures to be pipelined with design project work
Spr-Sum 78	Chapters 7, 8, 9 of text contributed by Chuck Seitz, H. T. Kung, Carver Mead
Jul 78	Chapters 1-9 of pre-publication draft completed for the upcoming MIT course

Sep 12, 79	MIT '78 course begins: 32 students plus a number of faculty observers
Sep 78	Hon, Sequin, Lyon complete "The Guide to LSI Implementation" for use in course design lab and for coordinating mask and fab.
Sep 78	Design lab setup: Dec 20 terminals, CIFTRAN symbolic layout software, HP pen-plotters.
Oct 24, 78	Design projects begin
Dec 6, 78	Design cut-off date: Student-project design files sent to PARC via ARPAnet (19 projects);
Dec 7-8, 78	Bell and Lyon merge files into 2 multi-project chip-types, convert to mask format.
mid Dec 78	E-beam masks made by Micro Mask, wafers fabrication begins at HP's Deer Creek Lab.
Dec 14, 78	Final class meeting
Jan 18, 79	Packaged design project chips returned to students at MIT for testing during the Independent Activity Period.

Innovating the ARPAnet-based "MPC" system for QTA prototyping of VLSI chip designs:

Early 79	Push-back against "toy" methods erupts both inside and outside PARC. Conway wonders "what to do?"
Spring 79	Conway invents MPC system for QTA prototyping of large numbers of chip-design projects (an early "internet commerce" system).
Summer 79	Conway goes for it: announces "MPC79"; Conway, Bell and Newell design and build prototype MPC system
Summer 79	Conway creates the "Guidebook for the Instructor of VLSI Design" from her detailed MIT lecture notes.
Aug 79	Hon, Sequin and Lyon complete 2nd edition of "The Guide to LSI Implementation"
Sep 79	Addison-Wesley publishes "Introduction to VLSI Systems", by Mead and Conway
Sep 79	VLSI courses start at 12 universities, using the Mead-Conway text, the Instructor's Guide, and the Guide to LSI Implementation
Fall 79	Conway, Bell, Lyon coordinate MPC79 events with faculty and lab assistants at the 12 universities
Dec 4, 79	MPC79 design cutoff: Bell gathers/merges all design files into 12 multi-project chip types on 2 wafer types
Dec 79	E-beam masks made by MicroMask, wafers fabricated by HP's Deer Creek Lab
Jan 2, 80	Packaged chips sent to the 12 universities: 82 projects, 124 designers, turnaround time: 29 days.
Jan 80	Fairbairn's and Rowson's new Magazine "Lambda" helps spread news of the stunning success of MPC79.
Spring 80	Group led by Ted Strollo at PARC initiates follow-on MPC580 project
May 30, 80	MPC580 design cutoff; all design files gathered/merged into many multi-project chips on 5 wafer types
Jun-Jul 80	E-beam masks made by MicroMask, wafers fabricated by HP's Deer Creek Lab
Jul 7-14, 80	Packaged chips sent to 15 universities/research-organizations: 171 projects, turnaround time (pipelined): 37-47 days.

Launching MOSIS by tech-transfer of the MPC system to USC-ISI:

Early 80	Bert Sutherland realizes that the MPC runs are a 'success disaster' for PARC; conceives of tech-transfer to USC-ISI
Spring 80	Sutherland, Conway, Bell (PARC) meet with Uncapher, Cohen, Lewicki (USC-ISI) to begin tech-transfer of MPC system
Early 81	The new MOSIS service begins operations, with funding from DARPA (and later from NSF)

Paradigm shift sweeps through in a flood of courses, EDA tools, chip architectures and startups:

Early 80	Bob Kahn and Duane Adams launch the DARPA VLSI Research Program
80-81	DARPA funds university researchers to build on the Mead-Conway methods, innovate chip architectures and EDA tools
Jan 81	Conway publishes "The MPC Adventures" as Xerox PARC technical report, reflecting on these events.
Oct 20, 81	Mead and Conway receive Electronics Award for Achievement, bringing wide notice to their work.
80 onward	Many short-intensive Mead-Conway VLSI design courses established (HP, VTI, Hellman Assoc., MIT, . . .)
80 onward	Foundry/broker startups begin providing QTA prototyping services (SynMOS, VTI, . . .)
81 onward	MOSIS-like organizations are launched in other countries (AUSMPC, CMP, NORCHIP, EIS, EUROCHIP, . . .)
82-83	113 universities around the world offered Mead-Conway courses by '82-'83 school year.
82 onward	Wave of startups begins (SGI, MIPS, SUN, ARM, . . . , Valid logic, Viewlogic, Mentor Graphics, Daisy, Cadence, . . .)
99	Impact of Mead-Conway methods and DARPA VLSI program documented in NRC book "Funding a Revolution"

Conway moves on to new fields:

81	Conway founds 'Knowledge Systems Area" at Xerox PARC; leads research in AI and collaboration technology
83	Joins DARPA as Assistant Director for Strategic Computing; leads research in machine intelligence
85	Joins University of Michigan as Professor of EECS and Associate Dean of Engineering

Conway's early IBM work uncovered; she finally 'comes out' to tell her story:

Dec 98	Conway stumbles onto Mark Smotherman's IBM-ACS website; realizes she must quietly come out.
99-Pres	Helps Smotherman locate ACS vets and reconstruct ACS history.
Nov 19, 00	Conway's story reported in L. A. Times article, "Through the Gender Labyrinth"
08	Conway begins building "The VLSI Archive"
Jan 10	Conway receives Computer Pioneer Award from IEEE Computer Society, in recognition of her early work
Nov 11	Conway publishes her ACS Reminiscences in Brian Randell's Festschrift
Dec 12	Conway publishes her VLSI Reminiscences in IEEE Solid State Circuits Magazine