**CDSC Year 5 Review and InTrans Award Kick-off Meeting**

**UCLA**

**54-134 Eng IV (Shannon Room) on Day 1, September 29, 2014**

**and**

**4760 Boelter Hall on Day 2, September 30, 2014**

**September 29, 2014 54-134 Eng IV (Shannon Room)**

**8:00am – 8:30am** ***Continental Breakfast*** **(53-125 Eng IV-Tesla Room)**

**8:30am – 9:15am** ***Opening Session***

* Welcome and Center overview, Jason Cong (UCLA CS & EE)
* Remark by Suzi Lacono, Director of NSF Computer and Information Science and Engineering Directorate
* Remark by Ricardo Suarez-Gartner, Director of University Research Office, Intel
* Remark by UCLA leadership

**9:15am – 10:15am *Application drivers***

* Thrust overview, Alex Bui (UCLA Radiology)
* CT reconstruction results for EM+TV, Will Hsu (UCLA Radiology)
* MR reconstruction and new compressive sensing-based approaches, Kyung Sung (UCLA Radiology)
* Computing challenges for genomics, Paul Spellman & Myron Peto (OHSU)

**10:15am – 10:40am *Break* (53-125 Eng IV-Tesla Room)**

**10:30am – 11:30am**  ***Customizable Heterogeneous Platform (CHP) Creation***

* Thrust overview, Glenn Reinman (UCLA CS)
* Accelerating genomic applications -- some initial experience, Yu-ting Chen (UCLA CS)
* Accelerator Interposed DIMM, Farnoosh Javadi (UCLA CS)
* Approximate Computing, Nazanin Farahpour (UCLA CS)

**11:30am – 1:30pm *Lunch* (53-125 Eng IV-Tesla Room)*+ invited talks from external visitors and collaborators***

* Three Ages of FPGAs, Steve Trimberger, Xilinx
* Back to the Future: The Incoming Wave of Innovation, Lynn Conway, Univ. of Michigan

**1:30pm – 2:45pm *CHP Compilation and Runtime Supports***

* Thrust overview, Vivek Sarkar (Rice CS)
* Data flow graph representation, Alina Sbirlea (Rice CS)
* On bounding the data movement complexity of algorithms, P. Sadayappan (OSU CS)
* Resource management in heterogeneous cluster computing, Hui Huang (UCLA CS)
* Distributed open community runtime, Zoran Budimlic

**2:45pm – 3:15pm *Break* (53-125 Eng IV-Tesla Room)**

**3:15pm – 4:30pm *Experimental Systems + Demo***

* Thrust overview, Jason Cong (UCLA, CS/EE)
* A heterogeneous computing cluster for big data applications, Bingjun Xiao (UCLA CS)
* Energy-efficient and reliable 3D CMOS/Memristor memory system - integration and optimization, Tim Cheng (UCSB, ECE)
* Potential impact to computing systems with multiband RF-interconnect, Frank Chang (UCLA, EE)

**4:30pm – 5:00pm *Poster introductions***

**6:00pm – 9:00pm *Poster session at UCLA Faculty Center-California Room (with dinner reception)***

**7:30pm – 8:15pm *Industrial Feedback to CDSC Research Programs (overlapping with poster session + dinner reception)***

**September 30, 2014 4760 BH**

**8:00am – 8:30am** ***Continental Breakfast***

**8:30am – 10:30am** ***Big data applications in personalized medicine***

* TBD, Gans Srinivasa, Intel
* Challenges and opportunities in data science in genomics, Wei Wang, UCLA CS
* TBD, Karthik Gururaj, Intel
* Batch-based FPGA acceleration of sequence alignment, Peng Wei, UCLA CS

**10:00am – 10:15am *Break***

 **10:30am – 1:00pm** ***Lunch + CDSC internal discussions***

* How to address feedbacks from the industrial visitors
* Plan under the InTrans program

**EXTERNAL SPEAKER BIOS AND ABSTRACTS**

**Back to the Future: The Incoming Wave of Innovation, Lynn Conway, Univ. of Michigan**

**Abstract:**

**Speaker bio: Lynn Conway** is Professor of Electrical Engineering and Computer Science Emerita at the University of Michigan. While at IBM-ACS in the 1960’s, Lynn invented ‘dynamic instruction scheduling’, a major advance in superscalar computer architecture. While at Xerox PARC in the 1970’s, Lynn invented scalable VLSI design rules, co-authored the classic text *Introduction to VLSI Systems* and pioneered the teaching of the new methods at M.I.T., launching a revolution in chip design. Lynn also invented and deployed the internet e-commerce system for rapid chip prototyping that became the "MOSIS" system, spawning the "fabless-design” and “silicon-foundry" paradigm of chip production. Currently affiliated with Michigan’s Center for Wireless Integrated MicroSensing and Systems (WIMS2), Lynn is a Fellow of the IEEE, a Fellow of the Computer History Museum, and a Member of the NAE.

**Three Ages of FPGAs, Steve Trimberger, Xilinx**

**Abstract:** Xilinx introduced the first FPGAs in 1984, though they were not called FPGAs until Andy Haines of Actel popularized the term around 1988.  Over the ensuing thirty years, the device we call an FPGA increased in capacity by more than a factor of 10,000 and increased in speed by a factor of 100.  Cost and energy consumption per unit function have decreased by more than a factor of 1000 (see figure 1).  These advancements have been driven largely by process technology, and it is tempting to perceive the evolution of FPGAs as a simple progression of capacity, following Moore's Law.  This perception is too simple.  The real story of FPGA progress is much more interesting.  FPGA devices have progressed through several distinct phases of development.  Each phase was driven by both process technology opportunity and application demand.  These driving pressures caused observable changes in the device characteristics, tools and business.  This talk is a retrospective on thirty years of FPGA technology and a forecast on the next Age of FPGAs.

**Speaker bio:**