*"If you want to build a ship, don't drum up people to collect wood and don't assign them tasks and work, but rather teach them to long for the endless immensity of the sea."* – Antoine de Saint-Exupéry

# MIT Reminiscences:
## Student years to VLSI revolution

By Lynn Conway, March 11, 2014 [Links updated: 1/31/15]

**A trip back in time: M.I.T. and the Charles River Basin as seen from Lynn's apartment in M.I.T's Eastgate, 1978.**
[Click on photos in these reminiscences to access higher-resolution images.]

There's always excitement in the air at MIT.

I first breathed that air in September 1955, as a 17 year old freshman moving into East Campus. As door after door of knowledge opened before me, I filled with feelings of empowerment.

Those feelings soon extended into everything I did, whether sailing Tech Dinghy's on a blustery day, or rock climbing in the Quincy Quarries, or later-on when exploring New England on a motorcycle.

Starting out in Course-8 (Physics) I did well, making High Honors Dean's List a number of times. But after taking the Course-6 (Electrical Engineering) circuits sequence, I became unsure of my goals.

Partly it was the magic of the time. A huge paradigm shift was underway in pulse and digital electronic circuitry, triggered by the WWII tsunami of innovation at MIT's Rad Lab.

I'd also been inspired by brilliant young EE instructors like Dudley Buck, who enabled us to visualize at a glance the behaviors of devices and circuitry we were playing around with inside our minds.

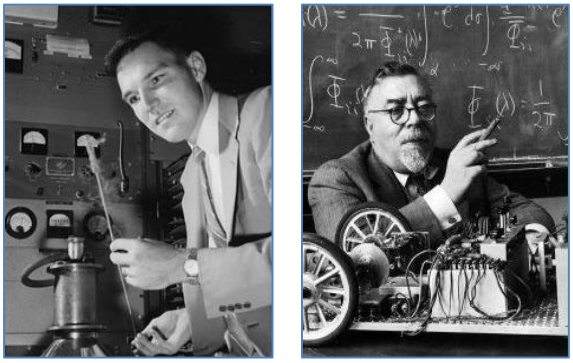


**Figure 1a,b: MIT's Dudley Buck and Norbert Weiner (1950's).**

Now, instead of seeing electronics as infrastructure for doing physics, I glimpsed a vast world for exploration, abstraction and meta-architectural innovation – an insight heightened by MIT's Norbert Weiner's visionary writings on "cybernetics."

I vividly recall Weiner trundling toward me one sunny day as I headed toward the Building 8 entrance. Although he was seemingly lost in thought, I tried to catch his eye, wondering what *he* saw inside *his* mind. Whatever it was, he was clearly still 'doing it' at an advancing age. A signal also rose above the noise: I was meant to do engineering after all.

But suddenly my whole world came crashing down. Unable to find any help, my intense efforts to resolve my lifelong gender-issues totally failed. Losing all hope of ever becoming a girl and living a meaningful life, I dropped out late in my senior year.

However, MIT had made its mark. I would instantly feel at home upon returning, two decades later.

**Getting it back together:**

Two years of back-room work repairing hearing-aids convinced me that a life of the mind would be better than no life at all. Living back at home in White Plains, N.Y., I butched-it-up and restarted my studies, this time in electrical engineering at Columbia University, commuting to the City by train.

Out of the blue, I became obsessed with digital computing – a wave just then rolling into Columbia's Electrical Engineering department with big-time support from IBM. Timing is everything, eh?

I got my BS, went on to my MSEE, had hopes of seeking a Ph.D., and took every computer-related course I could – from hardware design to computer architecture to numerical methods to advanced programming. I also began minoring in anthropology (yet *another* whole story).

Along the way, I did an independent study with Herb Schorr prior to his joining IBM Research. I must have made a good impression, and just in time: I couldn't survive on a TA's pay and desperately needed a job.

**In and out of IBM:**

Recruited in June 1964 by IBM Research, I soon found myself working for Herb on a secretive, highly proprietary, supercomputer project.

Advanced Computing Systems (ACS) had been launched by IBM CEO T. J. Watson, Jr., to create the world's most powerful scientific computer. Staffed with pre-eminent IBM experts, including the legendary John Cocke, the project moved in 1965 to what would become Silicon Valley. Over-stimulated by it all, I began making foundational innovations in superscalar computer architecture.

I also spotted another incoming wave. Innovative medical treatments had begun enabling successful gender transitions outside the U.S. (although society was hardly ready for this). With help from Harry Benjamin, M.D, I boarded the "trans underground railroad" in San Francisco and began my escape.

When I informed ACS's personnel department in 1968 that I was transitioning, word lurched to the top. IBM's Executive Committee (incl. T. J. Watson, Jr.) sent down their decision. I was fired.

A gritty survivor, I completed my transition in spring 1969, starting all over again in a covert identity as a contract programmer. It was a terrifying time. "Outing" could have led to becoming unemployable and cast onto the streets. Channeled by fear, I covered my past for decades – always looking over my shoulder – as if a foreign spy in my own country.

Simultaneously, I became so happy and productive that my career took off like a rocket. Recruited by Memorex, I climbed the ladder and soon got back into doing computer architecture.

**The big break:**

The break came in 1973: I was recruited by Xerox Palo Alto Research Center (PARC) just as it was getting underway.

It's hard to put into words the adventure that followed as PARC's community of researchers innovated, prototyped and evolved the modern form of networked personal computing, while working within the very techno-ecology they were jointly bootstrapping into existence.

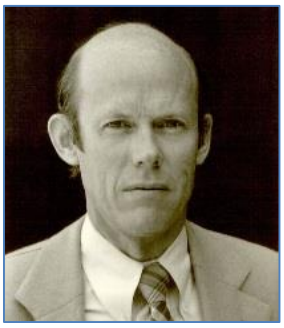
It was as if PARC were a throbbing meta-architecture generator, with feedback and gain in the system. Its rapidly evolving infrastructure enabled creative teams there to run circles around teams elsewhere, a full decade before such intellectual power-tools became more widely available.

**The onrush of complexity:**

Ivan Sutherland had joined Caltech in 1974 as Chair of its new CS department. Famous for his work in computer graphics, Ivan was excited about the potential of microelectronics. Carver Mead soon joined the department, bringing his expertise in device physics and circuit design and his connections in the semiconductor industry.

During 1975 Ivan, Carver, and Tom Everhart (then chair of EECS at Berkeley) conducted a major ARPA study of the basic limitations of microelectronics fabrication. Their report urgently recommended research into the system design implications of "very-large-scale integrated circuits" in light of predicted advances in lithographic scaling; no methods then existed for coping with such complexity and no approaches then underway held promise of solutions.

That same year, Bert Sutherland (Ivan's brother) joined PARC, managing the Systems Sciences Lab where I worked. He introduced me to Ivan and Carver. I began studying their recent investigations.



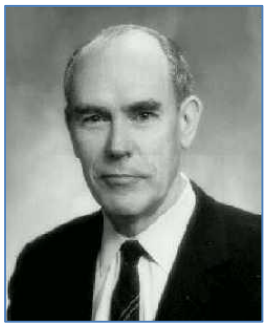


**Figure 2a,b: Bert Sutherland and Ivan Sutherland**

In January 1976, Ivan wrote Bert a now historic letter proposing that PARC and Caltech jointly attack the microelectronics complexity problem. Soon after, the Sutherlands established a formal collaboration between teams at PARC and Caltech, led by me and Carver respectively. Our mission: Innovate methods and tools that enabled digital systems to be more readily implemented in silicon, applying the personal computing infrastructure at PARC to the task.

The mystique of MIT deeply nourished these events: Both Ivan and Bert were MIT Ph.D.'s., having studied there under Claude Shannon; MIT's wildness had also infected me.

Going-meta, I went prospecting with PARC's culture in mind and its tools in hand – and stumbled right into the mother lode.

**Distilling the design methods:**

In a burst of activity, we all went to school on each other's knowledge and began patrolling for emerging practical knowledge across Silicon Valley. Peering down into the vast array of emerging-knowledge stovepipes, I looked for connectable wild stuff and distilled it as we went along.

As a consultant in device physics, Carver had learned Intel's NMOS circuit design methods. He'd also coined the term "Moore's Law" for the ongoing circuit-density scaling. Bruce Hoeneisen and Carver had also shown that the limit of MOS gate-length scaling was under 0.25μm. It followed that single chips would eventually contain tens of millions of transistors (turned out to be far, far more), rather than tens of thousands.

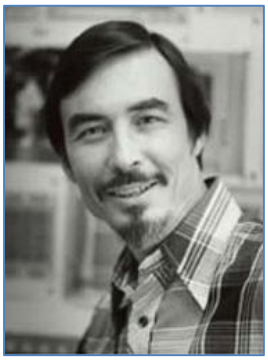


**Figure 3a,b: Lynn Conway and Carver Mead.**

Ivan had shown that with existing methods, interconnection wiring consumed increasing fractional-area as circuit density increased. This insight vectored us into composing digital systems using arrays of innovative MOS circuit cells on matching pitches.

Meanwhile, Doug Fairbairn at PARC and Jim Rowson at Caltech evolved *Icarus*, an Alto-based interactive layout editor, and we began using it for exploratory design. Mead's connections enabled him to occasionally fabricate a few projects from his Caltech NMOS circuit design courses. We followed that trail to fabricate research prototypes.

However, at the time the only way for a "writer" (a computer architect, like me) to commercially publish an "avant-garde novel" (an advanced microprocessor design) was to work inside a "publishing company" (a semiconductor manufacturer like Intel).

Moreover, Moore's law predicted that within a dozen years an ACS-like supercomputer would fit on a single chip, as would countless other complex systems yet to be innovated. But how on earth could a handful of semiconductor companies contain and channel the looming explosive-exponentiation of creativity and innovation?

Electrified by this techno-socio-political opening, I went on a mission to ensure the "freedom of the silicon press." ***Step one*: *bring the new language of VLSI design to the masses of potential writers.***

During a wild six-month period, Mead and I pooled our knowledge of integrated-circuit device-physics and digital-system architecture respectively. Reverse-engineering and re-assembling the existing hierarchy of digital-design abstraction-levels, we coalesced and distilled a minimalist design methodology that could quickly be acquired by system designers – folks skilled in the digital problem domain but lacking backgrounds in device physics and circuit design.

By exploiting dynamic NMOS logic for state-storage and using two-phase non-overlapping clocks to control register-transfers, we conceptually simplified and made transparent the expression in silicon of VLSI state machines and data paths.

I also invented a scalable set of digital layout design rules that remained "evergreen" as the semiconductor fabrication process scaled-down. It was the key that finally unlocked the puzzle.

Suddenly there it was: We'd distilled a minimalist but complete system of design knowledge that connected digital system architecture to scalable digital patterns in silicon. Better yet, the system digitally-interfaced design and manufacturing in a manner that echoed the laser-printing emerging at PARC.

We'd made a wild first ascent. Scrambling atop, I saw the grand walls of "VLSI Valley" looming ahead.

**The idea of doing "The Book":**

But what could we do with such knowledge? Write papers? Design chips?

Thomas Kuhn's insights had exposed the unlikelihood of launching such a paradigm-shifting *system of knowledge* by publishing bits and pieces in traditional journals or scattering fragments into commercial products.

In June 1977, I got the idea of *evolving a book in real-time* to coalesce and iteratively tune-up the evolving methods, using PARC's computers and information infrastructure to create, cohere, laser-print and share emerging results.

If cleverly crafted and filled with classical-looking working examples, such a book might "pass" as a text based on years of sound practice. And if it did pass, it might help trigger a paradigm shift. The concept wildly excited my colleagues.

In July 1977, I began writing the "Mead-Conway" text on my Alto at PARC, while stimulating inputs from Mead and contributions from team members.

Meanwhile, Ivan and Carver stimulated work at Caltech on an important design: the "OM2" microprocessor. As grad student Dave Johannsen strictly applied our emerging design methods to generate the OM2, I began exploiting its design throughout the book to convey the new methodological abstractions.

Importantly, I vividly knew my target-audience and how passionately they wanted into this game. They were computer architects, digital system designers and computer tool-builders, just like me.

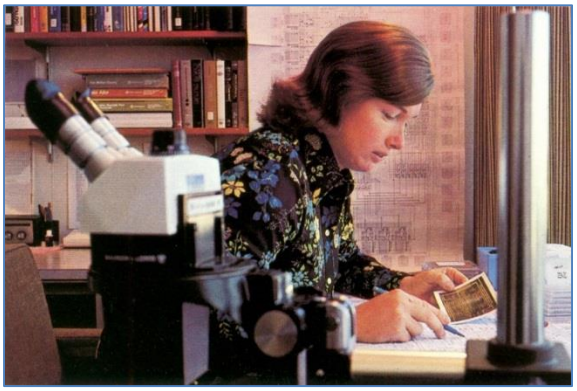


**Figure 4: Lynn at Xerox PARC (1977).**

**Bert's challenge:**

By coincidence, Bert Sutherland was on MIT's EECS department advisory committee. He soon offered me a challenge: "Go to MIT next fall and introduce a senior/masters-level course on this stuff." I was thrilled. We'd been testing parts of the book in a few *MOS circuit* design courses, but here was a chance to pioneer a *VLSI system* design course.

I was also terrified. Shy among strangers, fearful of public speaking, I lived in dread of being 'outed.' Sheltering in PARC's back rooms, I was virtually unknown outside. Teaching at MIT would be an overwhelming challenge. In my anxiety I wavered, but Bert insisted: "You've got to do this!"

Glancing at Charles Steinmetz's photo on my office wall, his story came back to mind. He'd launched the AC revolution by distilling and passionately teaching his methods at Union College. It was a turning point. I threw caution to the wind and went for it.

**Planning the MIT course:**

That spring I immersed myself in finishing the book. A full draft was ready by summer, just in time for the course. It included an open graphical standard for layout interchange, *CIF*, initially created by Ron Ayres and Ivan at Caltech, and was backed-up by a guidebook of distilled information on maskmaking and wafer fab by PARC summer-intern Rob Hon and PARC consultant Carlo Sequin of U.C. Berkeley.

Then it dawned on me: If I compressed the gist of the methods into the first half-semester, students could do design projects the second half. If I could then organize quick-turnaround (QTA) project fabrication, students could get chips back shortly afterwards.

Knowing MIT culture, I sensed that the unprecedented opportunity to design your own custom silicon chip would draw brilliant, intensely-motivated students. Their projects would, in turn, heavily test the design methods, the book, the course, the design tools and the QTA mask and wafer-fab methods. As summer progressed, I based the course syllabus on this schema.

Summer passed in a whirlwind of preparation. Before long I was packing-up boxes of freshly-minted, laser-printed VLSI texts and course handouts, and heading out on the 3000-mile road trip to MIT.

**Launching the MIT course:**

**Figure 5a,b: Research Laboratory for Electronics; Eastgate.**

Ensconced in a SW corner apartment high in Eastgate, I had great views out over the Charles River and MIT. While *How to Get Around MIT* (*HoToGAMIT*) helped me get back up-to-speed around the campus, the apartment was wonderful place to come home to, kick back and let my imagination roam.

Even so, launching the course was a formidable experience. I was terrified of becoming tongue-tied in front of the students. My solution was to be massively over-prepared. As the preplanned lecture sequence progressed, I wrote out each lecture in complete detail, including every instructional point, every drawing and every calculation.


**Figure 6: HoToGAMIT, 1978.**

Along the way, I unfolded the underlying generative concepts of electric circuit theory, electronic design, switching theory, logic design and computer system design so that all students became well-grounded in the gist of each level of abstraction, independent of prior backgrounds. With that shared knowledge in hand, they learned further details just-in-time while working on team projects.

I didn't see it coming at the time, but the effort to avoid gaps in student comprehension would have far-reaching impact. The accumulating hand-written lecture notes had captured its unfolding.

Jonathan (Jon) Allen was faculty host for the course and his grad student Glen Miranker was TA. Both went way beyond the call of duty to make it a success. The class included 32 students and 9 faculty/staff auditors. Researcher Bill Henke built a symbolic layout editor for encoding CIF layout specifications, while Glen set up a lab enabling students to access the editor via DEC20 terminals and plot layouts using HP pen plotters. Meanwhile, I coordinated with my team at PARC using a portable Texas Instruments printer-terminal to transmit e-mails via the ARPANET.


**Figure 7a,b: Jonathan Allen; Lynn's office in RLE.**

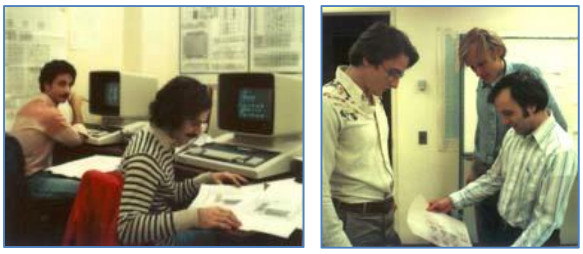


**Figure 8a,b: Students at DEC-20 terminals in VLSI design lab; Jim Cherry, Gerald Roylance, Glen Miranker study checkplot.**

Although primitively minimalist, the overall infrastructure was sufficient to bootstrap the course into existence – given the motivation, multi-disciplinarity and creativity of the overall assemblage of students.

**Framed with smoke and mirrors:**

Most students thought they were learning how chip design was done in Silicon Valley. The material seemed elegant and easy to visualize, so they delved in and filled their minds, not realizing they were using newly distilled (and not yet fully-validated) methods for chip design.

Some teams began expressing preexisting sorts of digital subsystems in NMOS. Others began riskier work to innovate architectural structures that creatively exploited the embedded topological properties of the technology. Excited competitions and collaborations developed as teams began their "creative writings." The gestalt was reminiscent of my mental efforts to exploit inside-knowledge of IBM's ECL integrated circuitry while exploring superscalar architectures years before at IBM-ACS.

However, some students also intuited that they were deeply embedded in an exotic MIT hack – and that if we pulled it off it would astonish the entire industry. As this wild concept sank in, they seized the moment. Hugely ambitious projects got underway. I held my breath. This could either blow up in our faces – or it could be huge.

**Launching the revolution:**

It was now time for techno-socio-political ***Step 2: show budding VLSI novelists how to print their works in silicon.***

By now, PARC researchers Dick Lyon and Alan Bell were well into preparations for QTA project implementation. Everyone pulled together at both ends to coordinate events as cut-off date approached.

On December 6, 1978, I sent the final design files to PARC via the ARPANET. Lyon and Bell merged projects and made masks at Micro Mask. Teaming up with Pat Castro at Hewlett-Packard, wafers were fabricated at her Integrated Circuit Processing Lab (ICPL) at HP Research, using a 6-µm NMOS process.

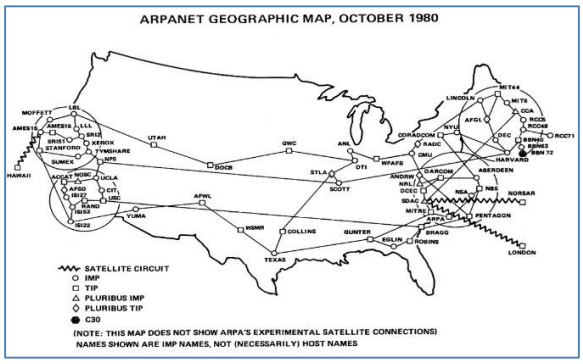



**Figure 9: Map of the early Arpanet (1980).**

It all went off without a hitch. Packaged chips for the 19 projects arrived at MIT on January 18, 1979, in time for students to test them during Independent Activities Period (IAP).

Although students had used minimalist early EDA tools, the new methods so regularized designs they made few errors. Thus began a rapid parallel evolution of new tools suited to the new methods.

For example, I used a chalkboard to track the projects' area requirements. As the deadline neared for merging designs into a multi-project-chip (MPC), I mounted scaled paper-cutouts on a whiteboard, rearranging them to minimize wasted area while juggling last-minute sizing contingencies. Out of context, those status-boards look like primitive hacks. However, by automating their novel functionality, I enabled a dramatic spread of MIT-like courses the following year.

**Figure 10a,b: Project Status Log; MPC Space Allocation.**

The course led to exciting projects. Jim Cherry designed a transformational memory for mirroring and rotating image data, and his chips were fully functional. Guy Steele even designed a complete LISP microprocessor! The machine almost worked on the first try, except for three small wiring errors, setting a high mark for architects to follow. But the overall set of projects had done far more. It had validated the prototype system of meta-architectural knowledge, in a symbiotically cybernetic sort of way.

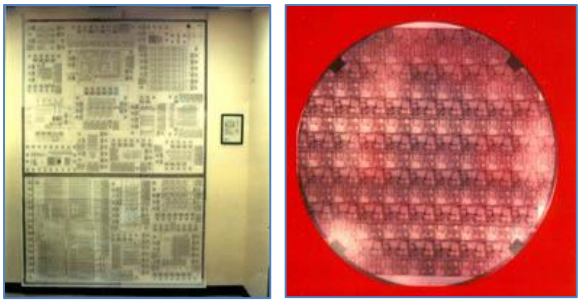


**Figure 11a,b: Wall-size checkplot of chipset; MIT'78 Wafer.**

After IAP, I took a leisurely route through the South and Southwest back to California. I knew something profound had happened, but had no idea where it would lead. I'd also gained confidence as a research leader and itched to do more. I drove on, rock music blaring on the radio, my head in the clouds, savoring the moment.

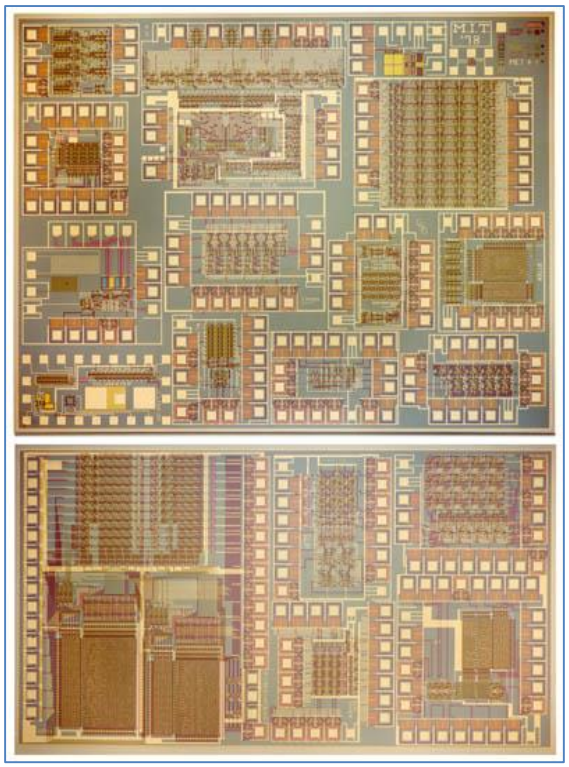


**Figure 12: MIT '78 chip set.**

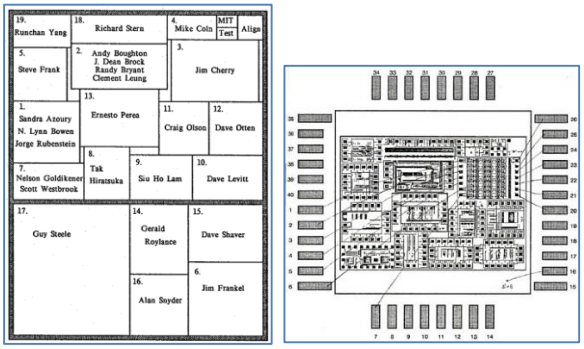



**Figure 13a,b: Project map; Wire bonding map for Project 3.**

**Figure 14: Class photo on final day of class.**

Something powerful also rode along on that road trip back to California: an *Instructor's Guidebook* on how to teach such a course, in the form of hundreds of pages of carefully-crafted handwritten lecture notes.

**Fallout, pushback, escalation:**

During the spring of 1979 (as I learned much later, in 2012), the explosive results of the MIT course were shared within an inner-elite of young turks at the "invitation-only" Asilomar Microprocessor Workshop (AMW5, 1979). Many were destined to later become Silicon Valley's leading industrial and academic figures. Carver Mead was one of them.

Uninvited and unaware AMW5 was even happening, I was clueless how the word had so quickly spread in elite circles. Even so, I sensed the resulting Valley tremors. Excited by that sensation, I raced to finish the book and get it published for courses the next fall.

However, disturbing signals of resistance also arose. Some in the TTL industry feared displacement if engineers began designing their own VLSI chips. Narrow over-optimizers in academia saw the simple-looking MIT projects as "toys" unworthy of making. Tribal pushback even arose within PARC. The book was headed into an establishment hornet's nest.

Grasping for straws, I pondered how to infect more schools with the MIT course just as the book came out. The *Instructor's Guide* provided the script, but how to fabricate so many projects?

It came to me in a flash: What if I created a server-based system to mediate logistics via the ARPANET? In a frenzy of activity, Alan Bell, Martin Newell and I lashed one together at PARC. The pioneering e-commerce system provided the scalability to support simultaneous QTA fabrication for multiple schools.

**Launching the MPC79 hackathon:**

That summer, I drafted a startling e-mail to ARPANET-connected research universities: if any ran MIT-like VLSI courses that fall, PARC would coordinate fabrications of their student projects. We called this hackathon "MPC79". Bert went along with the scheme, crossing his fingers every which way. Zoned on adrenalin, I steeled myself and hit "Send."

A dozen research universities took the bait. The MIT course had gone viral. Signals of resistance also grew louder. Rumor was that somebody named Conway had gone off the reservation, slipped up the river into Cambodia, and was spreading "unsound methods". If MPC79 didn't work my name would be Kurtz'ed.

Events climaxed on Dec. 4, 1979. We closed external interactions, and began die-layout planning for mask-making. Pat Castro again provided fabrication at HP, this time using a 5µm NMOS process. Packaged chips were shipped to designers on Jan. 2, 1980. The set contained 82 design projects from 124 designers. Astoundingly, turnaround time from design cutoff to packaged chips was only 29 days.

Many designs pushed the envelope of system architecture. Jim Clark, for example, prototyped the "Geometry Engine" and went on to launch Silicon Graphics based on the work. The designs weren't "toys" after all. An architectural gold rush had begun.

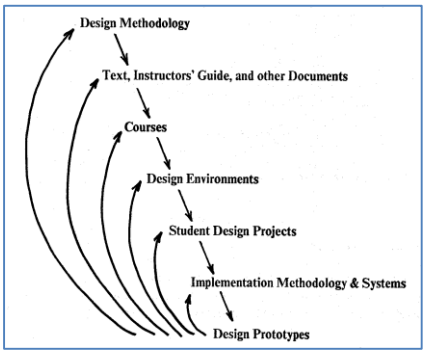



**Figure 15: The real-time evolution of a system of knowledge: Design prototypes provide feedback for evolution at all levels.**

**Exponentiation:**

The beauty of cool hacks is they stand by themselves. Like magic-tricks, what works, *works*! Even if folks have no clue *what* it is, *how* it works, or *who* did it.

**Figure 16: A classic MIT hack (2009); Solar-powered Red Line car circles the Great Dome's circumference.** *Boston.com*

During the spring of 1980, the MPC79 hackathon's hyper-explosive results were rapidly and privately shared among the young turks at AMW6. Although not a one ever talked to me about it, they now had no doubt. Whatever the heck was going on, it was real.

Back at MIT Chancellor Paul Gray grasped what had happened, and he noted on the record who'd done it.

Twelve universities had offered MIT-like courses in 1979; by 1982-83 the number totaled 113. The book eventually sold over 70,000 copies. Ever more authors wrote novels in the language of VLSI, editing their writings using the emerging EDA, then remotely printing them at what became known as "silicon foundries." Each resulting wave of digital machinery enabled the writing of more powerful novels. The resulting burst of courses, architectures, tools, chip designs and start-ups spawned an invasively-thriving, collaboratively-competitive, industrial ecosystem.

**Closure:**

This saga was about far more than just making digital systems. It was the exploratory launch of an evolving "meta-system of human-machine systems", one that internally-motivated a tumult of further tool-building and tool-use to opportunistically expand the envelope of the overall meta-system. There was gain in the cybernetic prototype. The rest is history.

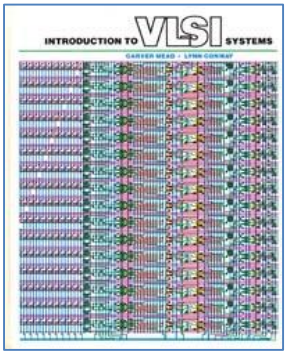



**Figure 17: The Mead-Conway text**
**Figure 18: Lynn Conway in her office at Xerox PARC (1983)**
*Photo by Margaret Moulton*

**Epilogue:**

I moved on to DARPA in 1983, then to the University of Michigan in 1985. Along the way I even got a life.

Meanwhile no one could explain the VLSI revolution, because down through the decades I'd quietly hidden away in the shadows – fearful of losing my career again if my past were uncovered. Folks simply took my elegant body of work for granted, and ran with it.

However, by 2012 the world had changed. Dave Hodges reached out and invited me to write a career-reminiscence for a special-issue of the *IEEE Solid-State Circuits Magazine*. I began unfolding the story in that special-issue, and have continued it here.

It all began at MIT, triggered by the excitement there in the 50's. Like a honeybee on a return flight, I felt compelled to bring some back in the 70's.

I've oft returned to walk MIT's corridors and breathe that air again. My most memorable visit was October 6, 2008, thirty years after launching the course. A beautiful fall day, a passing student captured the moment with my camera, out in front of Building 10.

**Figure 19: Lynn Conway at MIT, October 6, 2008**

Going back in, I climbed the stairs and peeked into 10-250. Seeing no one there I slipped inside, and took a seat high up in the great room where these adventures began in 1955. Replaying memorable physics lectures in my head, the magic lingered.

Got to run now – just spotted another incoming wave!

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**About the author:** Lynn Conway is Professor of Electrical Engineering and Computer Science, Emerita at the University of Michigan. A pioneer of VLSI microelectronics and a member of the National Academy of Engineering, she is currently affiliated with the Center for Wireless Integrated MicroSensing and Systems (WIMS2) at UofM. E-mail: Conway@umich.edu.

**Faculty Coordinator:** Professor Jonathan Allen; **Teaching Assistant:** Glen Miranker; **Design Lab Software**: William Henke,

**Students:** Sandra Azoury, Moshe Bain, Robert Baldwin, Andrew Boughton, Lynn Bowen, J. Dean Brock, Randal Bryant, James Cherry, Michael Coln, Martin Fraeman, Steven Frank, James Frankel, Nelson Goldikener, Tak Hiratsuka, Siu Ho Lam, Clement K. C. Leung, David Levitt, Rae McLellan, Craig Olson, David Otten, Ernesto Perea, Robert Reynolds, Gerald Roylance, Jorge Rubinstein, David Shaver, Alan Snyder, Guy Steele, Jr., Richard Stern, Robert Todd, Paul Toldalagi, Scott Westbrook, Runchan Yang

**Auditors, collaborators:** Dimitri Antoniadis, Fernando Corbato, Johan De Kleer, Clifton Fonstad, Jack Holloway, Syed Zaeem Hosain, Thomas Knight, Paul Penfield, Gerry Sussman, Richard Thornton

**Further readings:** *Lynnconway.com*, *M.I.T.'78 VLSI Course*, *VLSI Instructor's Guidebook*, *The MPC Adventures*, *The Design of VLSI Design Methods*, *Towards the Principled Engineering of Knowledge*, *The VLSI Archive*, *Hacks at MIT*, *Lynn Conway's VLSI Reminiscences*, *The VLSI Revolution at MIT, by Paul Penfield* (*2014 EECS Connector, pp.11-13*), *Envisioning the Adventures Ahead*, *The Incoming Wave of Innovation*.