

Transcription of Lynn Conway's Plenary Talk During the ERI Panel-Session at DARPA's 60th Anniversary Symposium, September 5, 2018



Many thanks for the introduction Bill ([Bill Chapell](#), Director of DARPA/MTO). It's such a thrill to be here at [DARPA's 60th](#) as we reflect on where we've been and ponder where we're headed.

As background for our panel, I'll give an overview of [DARPA's pivotal role](#) in the [VLSI revolution](#), and how the new VLSI technology and [ARPAnet](#) began synergistically co-evolving in the late '70s. We've enjoyed four decades of breathtaking progress ever since. What a trip it's been.

With the plateauing of [Moore's Law](#), many folks see the roads ahead blocked by looming complexity. In great contrast, we envision exciting break-outs into vast unexplored territories.

The Reason? As an old-timer at 80, I've lived through something like this before. Namely the 'complexity bind' facing microelectronics in the mid-70s. Lessons learned back then seem directly applicable now.

So let's go on a trip down memory lane, starting in '75 just BEFORE the VLSI revolution.

Microprocessors contained ~7,000 transistors. In the fab houses, specialists in computer architecture, logic design, circuit design, circuit layout and process design worked inside separate silos of expertise on overall chip design. As each specialty independently optimized its work, overall complexity grew by leaps and bounds.

EX: circuit layout involved using ~40 pages of complex design-rules when crafting huge hand-carved, hand-checked rubylith artworks – which were photographically reduced to make reticles and masks.

[Dennard Scaling](#) suddenly exposed an incredible possibility. Given Moore's Law, working chips might contain a million transistors by ~1990. But no means existed for designing such complex chips. It was as if printing had been invented before written language!

In a wild burst of collaborative research at Xerox PARC and Caltech, we evolved a set of 'structured VLSI design methods', displacing over-optimized traditional specialties. For example, at one abstraction level, we invented concise, scalable layout design rules (**See Fig 4**). Usable in simple EDA tools running on personal workstations, they provided a precision digital interface between design and fab.

The overall 'Mead-Conway' methods enabled even novices to do top-to-bottom architecture and design of silicon systems. We drafted a textbook on the methods using PARC's ALTO personal computers and laser printers, then used it to launch an [experimental VLSI Design course](#) at MIT in the fall of '78.

Students quickly grasped the new methods and did chip projects that were fabricated at HP Labs afterwards. The results of this new form of "fabless design" included a LISP microprocessor by Guy Steele and stunned the industry. Many other schools wanted to offer "MIT VLSI courses". I struggled with how to scale the experience.

This led to conception of what we now call an "e-commerce system" enabling students to send design files via the ARPAnet to a "remote server" at PARC. Server software packed them into files for e-beam masks for multi-project wafers (MPWs) to be made in a "silicon foundry" (as they became called). Here's what the software looked like (**See Fig 9**).

Taking a huge risk, my little team at PARC announced to major research universities "if you offer Mead-Conway courses, PARC and HP will fab your student projects". 12 schools took the bait. What became known as "MPC79" exploded into a wild "ARPAnet happening" that fall (**See Fig 11**).

In early December, 129 students and researchers sent in scores of innovative designs. Chips were returned from HP Lab's "foundry" in early January 1980. One was the prototype "[Geometry Engine](#)" by Jim Clark, leading to the founding of Silicon Graphics (SGI).

[MPC79 demoed and validated](#) the VLSI design methods, book, courses, EDA tools and e-commerce system. Running at scale and in sync, it bootstrapped a VLSI techno-social ecosystem.

In '80, DARPA founded the VLSI Program to support explorations in this new frontier. In '81 we transferred the MPC79 technology to USC-ISI, where it was supported as the "[MOSIS](#)" service by DARPA. By 1983, VLSI courses were offered at [113 universities](#). Moore's Law held. Modern VLSI chips contain complex systems of billions of transistors.

Let's now take a closer look at Fig 11 and envision the symbiotic co-evolution of VLSI and ARPAnet. At each major iteration of this techno-social system, VLSI chips embedded in computer workstations and ARPAnet routers and servers enable the design of VLSI chips for more-powerful workstations, routers and servers. The game's then rerun, using the next-node's VLSI chips. The dramatic results mirrored the synergistic exponentiation of railroads and telegraphy in the 19th century.

Reflections and Lessons Learned

The accumulation of local complexity is akin to 'hoarding'. It continually wastes both human-and-machine time-and-energy. Needless complexity should be continually deconstructed.

Upon simplification, specialties are more easily cross-visualized. Teams can see each other's forests for the trees. Cross-cutting, disruptive innovations are more rapidly made and disseminated.

In all this, open team competition is a vital form of collaboration. It makes visible and helps select innovations that improve the overall game.

Such 'techno-social dynamical processes' involve humans and their tools within all feedback loops ... thus innovations in 'user-experiences' are central to their empowerment.

And always remember: Narrow expertise has a half-life, and it gets ever shorter in times of accelerating techno-social change. As philosopher [Eric Hoffer](#) said:

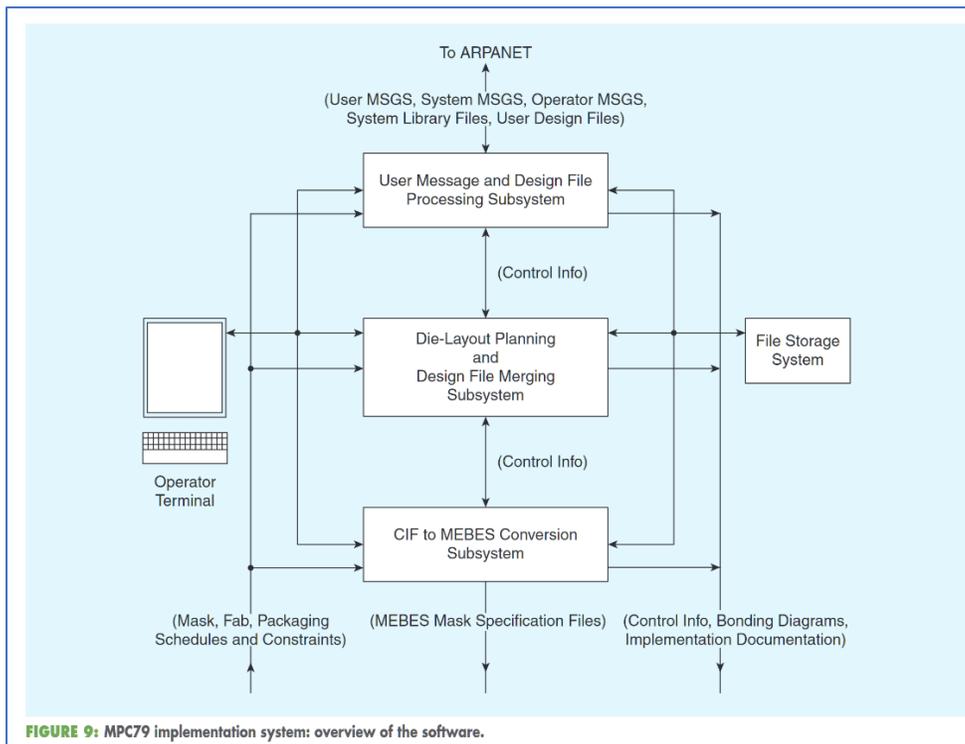
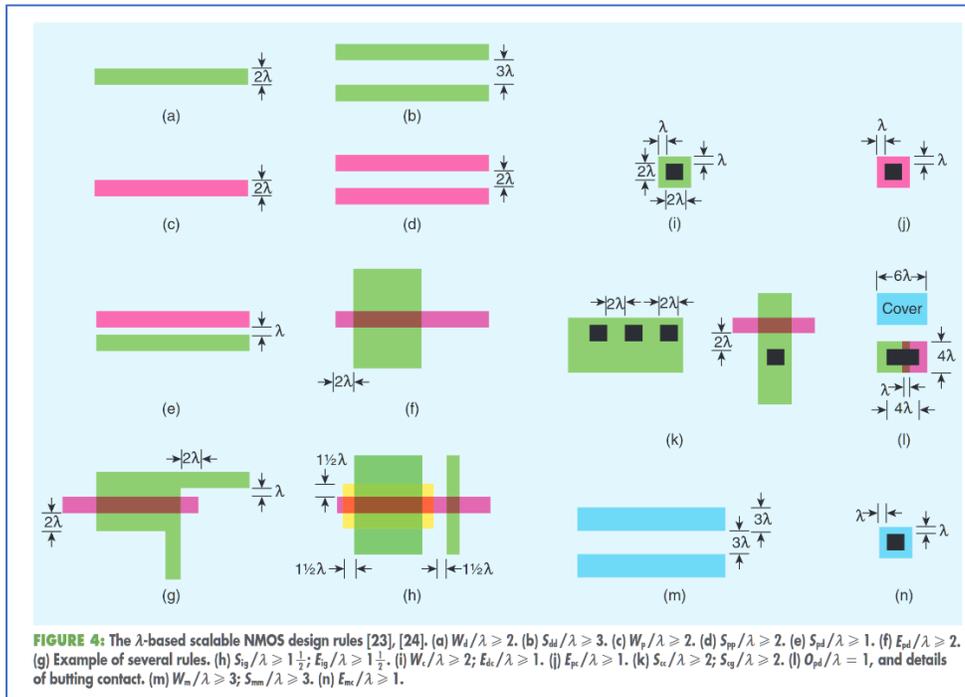
"In a world of change, the learners shall inherit the earth, while the learned shall find themselves perfectly suited for a world that no longer exists."

Thank you!

Reference:

1. L. Conway, "Reminiscences of the VLSI Revolution: How a Series of Failures Triggered a Paradigm Shift in Digital Design," *IEEE Solid-State Circuits Magazine*, vol. 4, no. 4, 2012, pp. 8–31.
http://ai.eecs.umich.edu/people/conway/Memoirs/VLSI/SSCM/VLSI_Reminiscences.pdf

Slides (Figures from Reference 1):



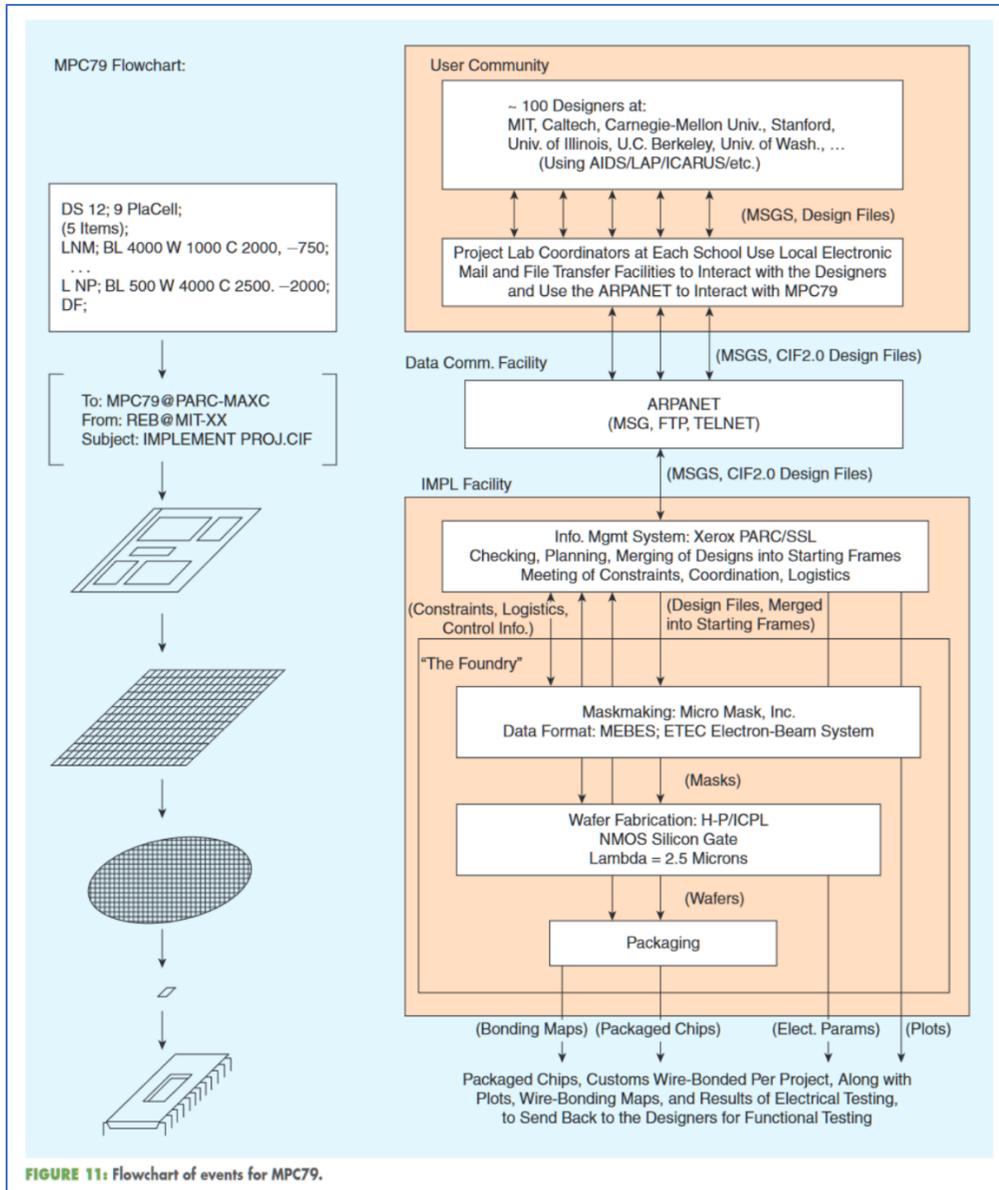


FIGURE 11: Flowchart of events for MPC79.