MEMOREX 7100

I/O SYSTEM

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CONTENTS

FIGURES

1.0 INTRODUCTION

This section will discuss the 7100 I/O Subsystem. The I/O Subsystem has been designed to make maximum use of CPU resources. The I/O Subsystem consists of peripheral devices that are connected to the CPU and main memory through control units that are integrated into the mainframe design. These integrated control units, or adapters, are directly controlled by a common micro-processor in the CPU.

2.0 7100 I/O ARCHITECTURE

Peripheral devices on the 7100 System connect to the system through integrated adapters (control units). These adapters are controlled by the micro-processor in the CPU and make use of common resources in the CPU such as ALU, address and data registers and a scratch pad memory used as a register file.

Figure I outlines the basic interconnection of integrated adapters to the system. All I/O adapters connect to the micro-bus. The micro-bus provides basic control to the adapters for I/O initiation, termination and data transfer. The exceptions to this general rule are the disc adapter and the selector channel adapter, which, due to their high rate of data transfer, go directly to the memory bus for data transfer.

Each peripheral I/O adapter is assigned a processor state as seen in Figure II. Each processor state is assigned a column in the system register file. The system register file contains registers

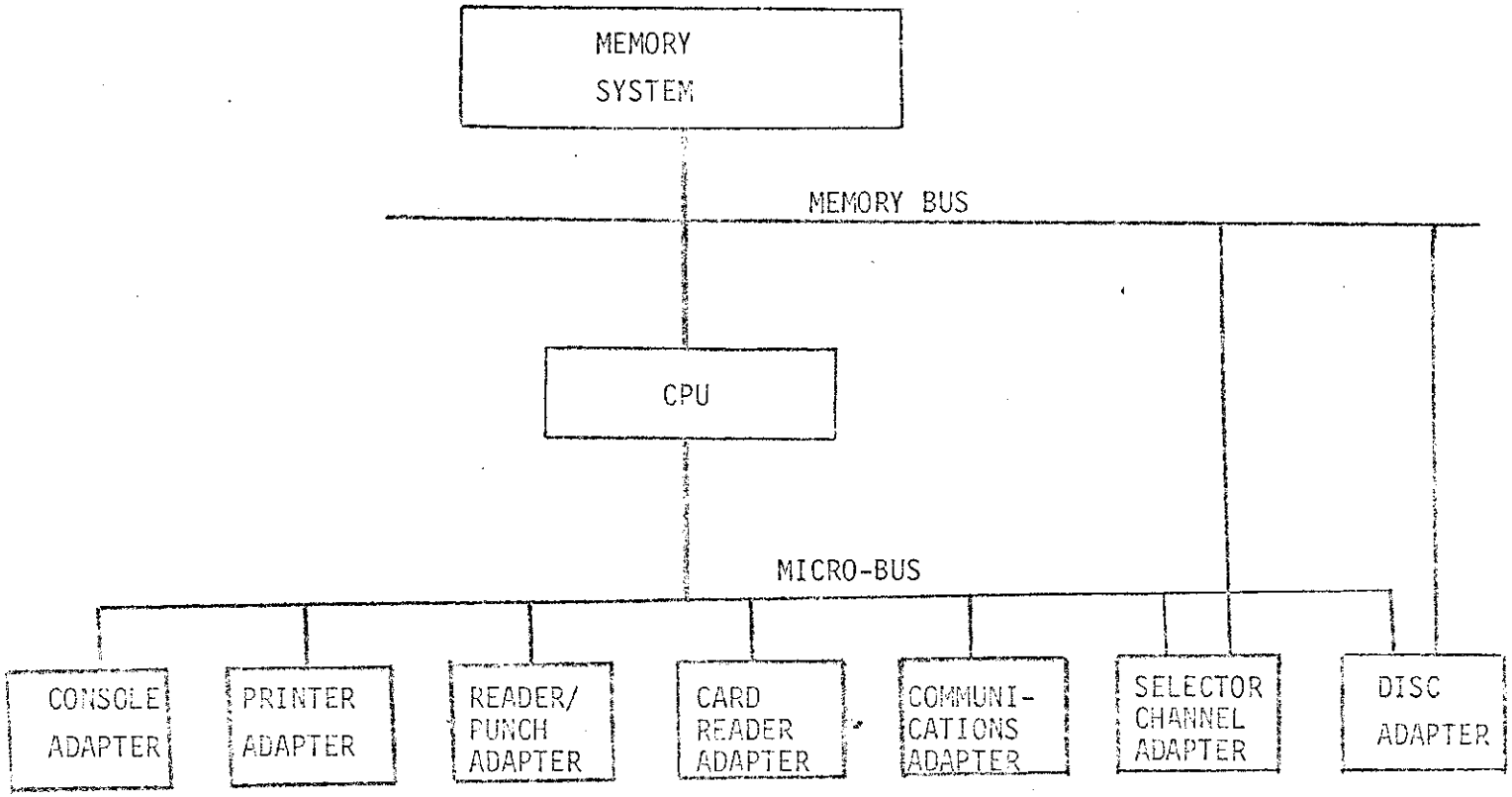


FIGURE I

INTEGRATED ADAPTER INTERCONNECTION TO 7100 SYSTEM

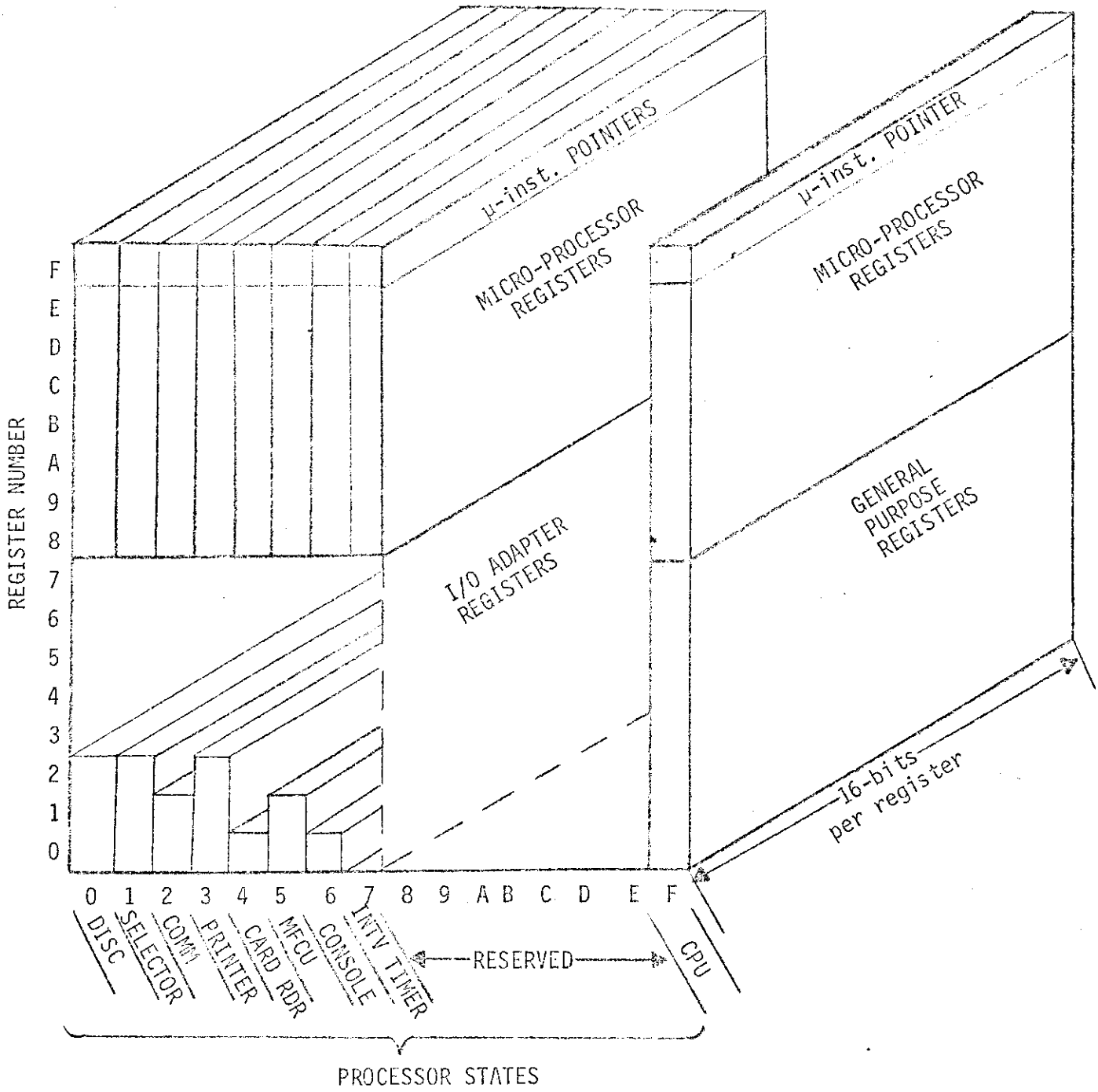


FIGURE II

7100 SYSTEM REGISTER FILE

8-F in Columns 0-7 and 0-F in Column F. Columns 8-E are reserved for future use.

Each I/O adapter has varying numbers (up to 8) of discrete registers located in the adapter. These registers can be addressed by the micro-processor as though they were located in the system register file. Thus, the micro-processor has 8 working registers plus up to 8 discrete adapter registers for each I/O processor state.

Register F is reserved in each processor state for the micro-processor program counter. Thus, each time a processor state change occurs, the entry point in the micro-program is obtained from Register F of the newly selected state.

2.1 Integrated Adapters

Integrated adapters on the 7100 System provide data buffering and control to the peripheral device. Because different types of devices have different characteristics, adapters are designed specifically to meet the needs of each type of peripheral device.

Figure III shows grossly what is required for most types of adapters. Each I/O device requires a certain amount of discrete logic to control it. This, in general, is in the form of latches that set and remember commands or conditions during an I/O operation. During data transfer, buffering of data is required between the I/O device and the CPU or memory. Each adapter must have logic to sequence the work flow through the adapter, (i.e., moving data in and out of the adapter, requesting CPU service, etc.).

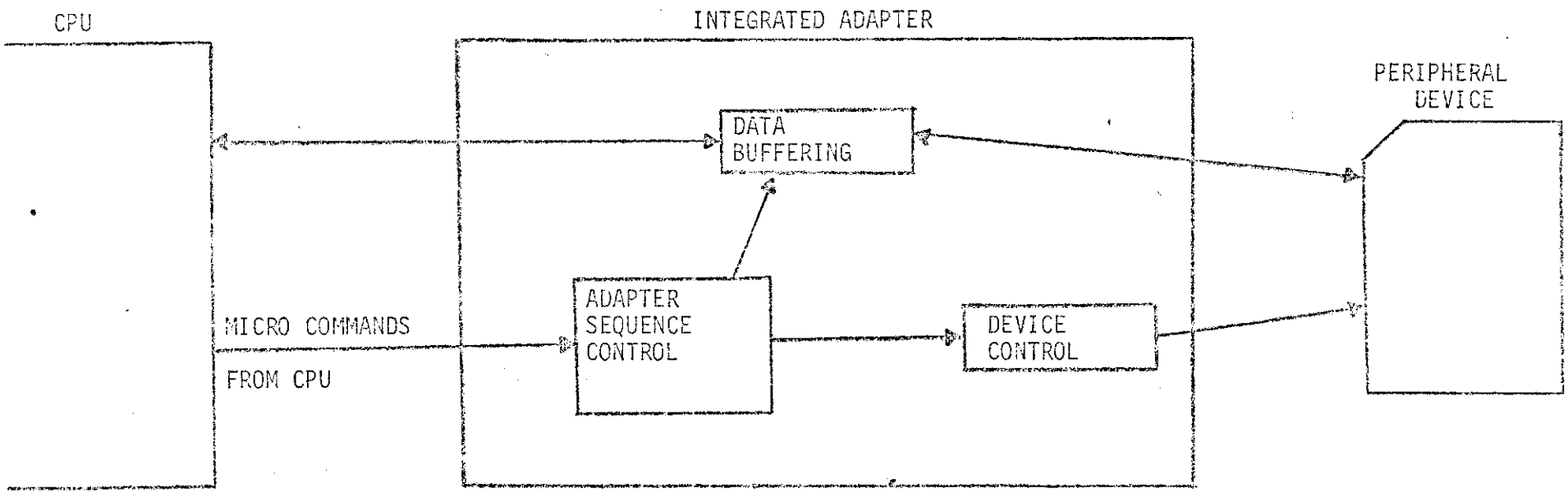


FIGURE III

INTEGRATED ADAPTER BLOCK DIAGRAM

In the 7100 System, the adapters are passive in nature and depend on the micro-processor to control them. In certain cases where the micro-processor is not fast enough to respond to peripheral needs (eg. serialization/deserialization of bit stream data on disc storage devices) discrete logic is provided in the adapter to perform these functions. In general, when a status change takes place in an adapter, the adapter requests service from the micro-processor and waits for the micro-processor to respond. Examples of this will be covered in Section 2.4, Micro-Processor Control of Adapters.

All I/O adapters contain certain common elements such as registers to hold status, device commands and buffer data. These registers are directly accessible by the micro-processor which can read or write these registers. In addition, the micro-processor can issue certain commands that cause the adapter to perform a function, such as, master clear, drop request line, initiate operation to device, etc.

2.2 Micro-Bus Interface

The micro-bus interface provides the vehicle to initiate I/O operations, transfer data and terminate I/O operations.

Figure IV shows a diagram of the micro-bus interface. This interface consists of:

1) Bi-directional, 16 bit Data Bus

This bus interfaces between the registers in the CPU (i.e., MDR, A feeder, B feeder, etc.) and one of eight registers in the adapter.(NOTE: Most adapters only require 2 or 3 registers.)

2) Register Address Line

These lines decode off of the micro-instruction register source and destination fields and select one of eight registers referred to above as Item 1.

3) Read/Write Lines

The read/write line signals the I/O adapter whether the selected register is to be a source or destination. The read line indicates a source, the write line indicates a destination.

4) Adapter Select Lines

These lines select 1 of 8 possible I/O adapters. I/O adapters should respond to signals on the micro-bus interface only when their assigned address is present on the adapter select lines.

5) Service Request Line

Each adapter has a unique service request line. The service request line is used by the adapter to signal the CPU that it needs the services of the micro-processor. At an appropriate time, the CPU will use the service request line, through a priority network to select a new CPU state which will affect the adapter select lines.

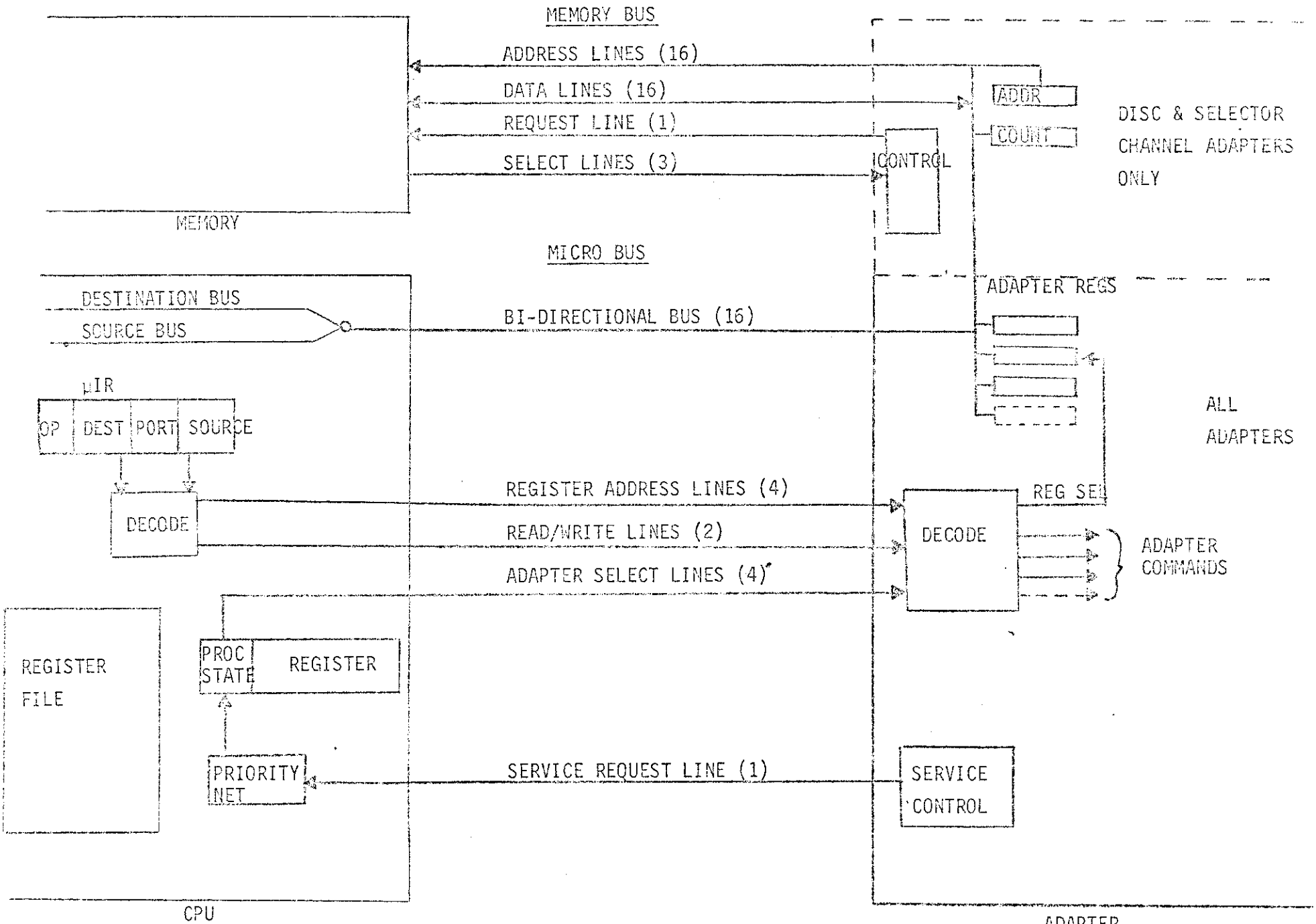


FIGURE IV

DETAILED ADAPTER - CPU INTERFACE

2.3 Memory Bus Interface

The memory bus interface is used by certain adapters that have high speed (> 27K byte) data transfer requirements such as the disc storage unit and the selector channel.

The memory bus interface consists of:

1) 16 Address Lines
2) 16 Data Lines
3) 1 Request Line per Adapter
4) 3 Select Lines

Refer to "Memorex 7100 Memory System" description for timing and interfacing requirement.

2.4 Micro-Processor Control of Adapters

The micro-processor, as described in previous sections, can access registers in each of the adapters on the 7100 System. In addition to loading and reading these adapter registers, the micro-processor can instruct the adapters to perform certain progammed sequences.

These instructed sequences from the micro-processor can be interpreted in two ways. One, the act of loading adapter registers can be used by the adapter to initiate certain operations. For example, assume that one register in the adapter is assigned to be a command register for a peripheral device, then, the act of loading the register could signal the adapter to start a procedure with the peripheral device, the exact operation being dependent on the content of the register just loaded.

Another method of instructing the adapter can be through the use of register address decodes of registers not present in the adapter. For example, assume that a particular adapter has 3 discrete registers. Since each adapter has an addressable range of 8 registers, 5 register addresses would normally be unused. If these unused addresses were decoded and interpreted by the adapter as commands then 10 unique (5 read and 5 write) instructions would be decoded through normal microprogram access to adapter registers. Refer to adapter decode block in Figure IV.

During a normal I/O sequence at the point of I/O initiation the system will switch to the processor state associated with the pertinent adapter (see Figure II).

The micro-processor will access memory to obtain the"command word" which describes the I/O operation that is to take place. The micro-processor will make any necessary error checks for format and content of the "command word." If no errors are detected, the micro-processor will begin an I/O command sequence with the adapter.

Once the operation is underway, the micro-processor will relinquish control to another processor state until data transfer is required (this time varys with the peripheral device).

When the adapter detects that an access to memory is eminent, it will raise the service request line to the micro-processor priority network.

In due time, the micro-processor will respond by again switching to the processor state for the requesting adapter. Because the micro-program initiated the I/O operation, it usually knows what type of response will be required to an ensuing request and will have the micro-program counter pointing to the proper (i.e., read or write) micro-program routine.

Once the switch has taken place, the micro-program will access memory and send the data to the adapter data buffer (write sequence) or access the adapter data buffer and send the data to memory (read sequence). In either case, the micro-program will update the memory address pointer and the data block counter. The micro-program will detect for end of block. If the end of block specified by the "command word" and the end of record specified by the peripheral device do not coincide an error status condition will occur.

After each byte of data is transferred, the micro-processor relinquishes control to another processor state.

When all of the requested data has been transferred, the micro-program goes through a clean up procedure to terminate the I/O operation. If command chaining was requested by the "command word" in memory, the micro-program will access the next "command word" and the procedure starts all over again.

2.5 I/O Timing Consideration

1) Adapter Selection Address Lines

The 4 adapter selection address lines indicate to the I/O adapter which block of extended registers the processor wishes to communicate with. The 4 lines make it possible to address 16 separate register blocks. These address lines must be stable 130 n sec. after the trailing edge of the system clock for a write request and 90 n sec. after the trailing edge of the system clock for a read request.

2) Register Address Lines

The 4 register address lines indicate to the I/O adapter which register in the block of extended registers the processor wishes the address. The 4 lines make it possible to address 16 different registers. The address line must be stable 170 n sec. after the trailing edge of the system clock for a write request and 130 n sec. after the trailing edge of the system clock for a read request.

3) I/O Write Line

The I/O write line indicates to the I/O adapter that the processor wishes to perform a register write function. The write line must be stable 130 n sec. after the trailing edge of system clock.

4) I/O Read Line

The I/O read line indicates to the I/O adapter that the processor wishes to read the contents of a register. The read line must be stable 130 n sec. after the trailing edge of system clock.

5) Micro Bus

The 16 line micro bus is a bi-directional communication link between the processor and the I/O adapters. In a write operation, the I/O adapter must have the bus stable 170 n sec. after the trailing edge of system clock. In a read operation, the bus will be stable 230 n sec. after the trailing edge of system clock.

3.1 EIGHTY COLUMN CARD INTEGRATED READER PUNCH ADAPTER (IRPA80)

3.1.1 GENERAL

The IRPA80 is the Integrated Adapter/Controller which contains the hardware interface and control logic required to operate the MRX 8205 Card Reader Punch (Control Data Corp. Model 9280). The IRPA80 may also be used as the Adapter/Controller for MRX 8010 models 1, 2, and 3 (Documation Inc., models M300L, M600L, and M1000L).

3.1.2 PERIPHERAL DEVICE DESCRIPTION

3.1.2.1.1 The CDC Model 9280 will both read and punch eighty column cards in one pass. It is capable of reading at 500 cpm or punching at 100 cpm. The Model 9280 consists of a column oriented, card read-punch unit complete with Hopper, Stacker, internal Control Unit, and Power supply.

3.1.2.1.2 The Model 9280 uses fiber optics to accomplish the photo-electric reading. The read system is resynchronized on each punched column to insure reliable reading of "old" or mutilated cards. An added feature is the punch "Skip-Out" capability which allows a card to be fed at transport rates after the final desired column is punched. It also has a stacker card "Offset" capability.

3.1.2.2.1 The Documation M Series readers will read eighty column cards, column-by-column. The M300 L reads at a rate of 300 cpm, the M600L reads at 600 cpm, and the M1000L reads at 1000 cpm.

3.1.2.2.2 The M Series Mechanisms consist of a Hopper, Read Station, and stacker. All units use long-life LEDs to accomplish the photo-electric reading.

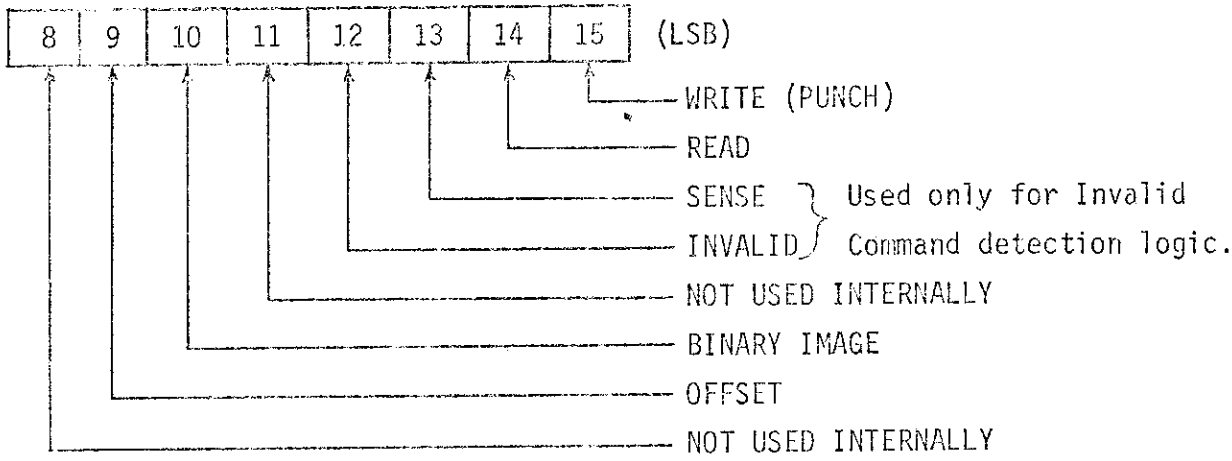
3.1.3 IRPA80 DESCRIPTION

3.1.3.1 The Eighty Column Integrated Reader-Punch adapter logic is contained on two plug-in boards. This logic is divided between a "Register" board and a "Control" board. The IRPA interfaces to the micro-processor via the I/O micro-bus, the row and column address lines, the read/write control lines, and the service request line. For additional information on the I/O interface, refer to Section 2.0.

3.1.3.2 IRPA80 Register Board

The IRPA80 Register Board contains the Command Register, Invalid Command detection logic, Punch Data register, Input Data register, Hollerith conversion logic, and Hollerith Validity check logic. (Refer to IRPA80 logic diagram or Block Diagram 3.1.4)

3.1.3.2.1 The Command Register is 8 bits in length. During the I/O initiation procedure the micro-processor fetches the Command Byte from the SI/O instruction and loads it into this register. The Command Byte is then available to the micro-processor for testing and, normally, will remain in the command register for the duration of one I/O operation. The bits in this register correspond to bits 8 thru 15 of the micro-bus and their meanings are assigned as follows:



3.1.3.2.2 The Invalid Command Detection logic tests the four least significant bits of the Command register. Three of the sixteen possible combinations will be sensed as an invalid command. These are:

1) 0000 Invalid
2) 1000 Transfer in Channel
3) 1100 Read Backward

The Invalid Command term is one of the inputs to the Command Reject logic on the Control board. However, the Invalid Command term will not cause a "Command Reject" to occur unless it is present when the micro-processor executes a "Start I/O" (TEED) control function.

3.1.3.2.3 The Punch Data Register is the outbound data buffer during Card Punch operations. It is 12 bits in length, and they correspond to bits 4 thru 15 of the micro-bus. This register is loaded by the Write Decoder "Load Punch Data" term. The register outputs are connected to the inputs of the EBCDIC/Hollerith ROM converter. A punch multiplexer is used to select either the converted hollerith character or the Punch register outputs (bypassing the converter logic) and to present the resultant Punch data to the peripheral interface. The punch multiplexer data selection is controlled by the Binary image bit of the Command register. Either an "Image" character or a "converted" character is always present on the Punch Data lines. This Punch Data is also available to the Input Multiplexer, thus providing the capability for diagnostic testing of the outbound data paths.

3.1.3.2.4 The Input Data Register is the inbound data buffer during Card Read operations. It is 12 bits in length, and they correspond to bits 4 thru 15 of the micro-bus. Normally, this register is loaded with data read from one column of the card in the device read station, and is loaded on the leading edge of the Busy signal (data index) from the peripheral device. This register may also be loaded from the micro-bus, thus providing the capability for diagnostic testing of the inbound data paths. The register outputs are connected to the Hollerith/EBCDIC conversion logic. A Binary Read multiplexer is used to select the converted EBCDIC character or the Input Data register (bypassing the converter logic) and to present the resultant input data to the Input Multiplexer.

3.1.3.2.5 A Hollerith Validity Check is performed on inbound data if the IRPA is not in Binary Image mode. The Validity check logic inputs are connected to the seven least significant bits of the Input Data register. If more than one of these seven bits is set, the Hollerith Valid term will be not true. If the Hollerith character is not valid, and the IRPA is not in Binary Image mode, the Data Check flag will be set.

3.1.3.3 IRPA80 Control Board

The IRPA80 Control Board contains the Read Control and Write Control decoders, the Input Multiplexer, the Data Transfer Control Logic, Data Check logic, Adapter Status logic, and the Peripheral Device Status logic.

3.1.3.3.1 In order to perform an I/O operation related to the IRPA80 or the attached peripheral device, the micro-processor must first establish the correct Column Address to select this Adapter. The micro-processor must then execute an I/O micro-instruction: which will establish the I/O Row Address for the register, or control function, desired; and which must raise either the I/O Read signal to specify that the IRPA80 is the information source, or the I/O Write signal to specify the IRPA80 for a control function or as an information destination.

3.1.3.3.2 The I/O Row Address is presented to the Read Decoder, the Write Decoder, and the Input Multiplexer. The Input Multiplexer selects the information specified by the I/O Row Address and, if it is a Read operation, the output drivers are enabled, placing the information on the I/O micro-bus. The selected information is one of the following:

1) Input Data (sourced from the Input Data register or the Hollerith/EBCDIC converter)
2) Punch Data (sourced from the Punch Data line)
3) Command Byte (sourced from the Command register)
4) Status (Attention, Busy, Device End, Unit Check, Request In)
5) Sense (Command Reject, Intervention, Data Check, Overrun, Not Ready, Device Status, CPU Data Request)

3.1.3.3.3 The Write Decoder is enabled by the I/O write term and, depending on the Row Address contents, decodes one of the following Register Load or Control Function terms:

1) Load Input Data (register load)
2) Load Command Byte (register load)
3) Load Punch Data (register load)
4) Start I/O (control function)
5) Halt I/O (control function)

6) Clear Status (control function)
7) Reset Device (control function)

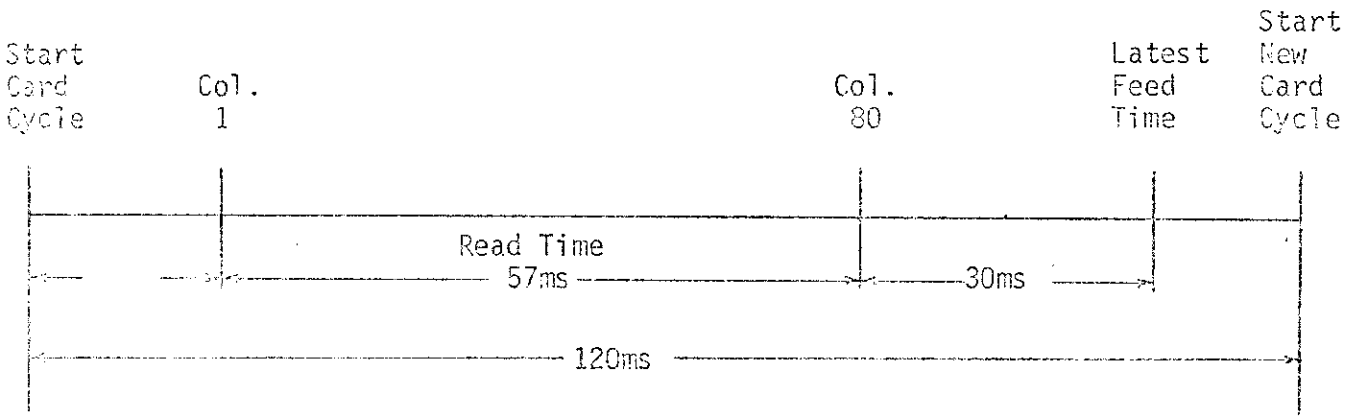
3.1.3.3.4 There is one Write address function and three Read address functions not used by the IRPA80. These are interpreted as illegal addresses and, should the micro-processor attempt to execute one of these when the Column Address is pointing to the IRPA80, the Command Reject Flag will be set to indicate an error condition.

3.1.3.3.5 The Active Flip Flop is set if the peripheral device is "Ready" and the micro-code issues a Start I/O control function to the IRPA80. It is reset by the Halt I/O control function. When the Active FF is reset, all service requests are inhibited except "Attention". Also, all data transfers between the IRPA80 and the peripheral device are inhibited. However, all Control functions and data transfers between the IRPA80 and the micro-processor are allowed in order to provide for diagnostics, adapter testing, and I/O initiation/termination procedures.

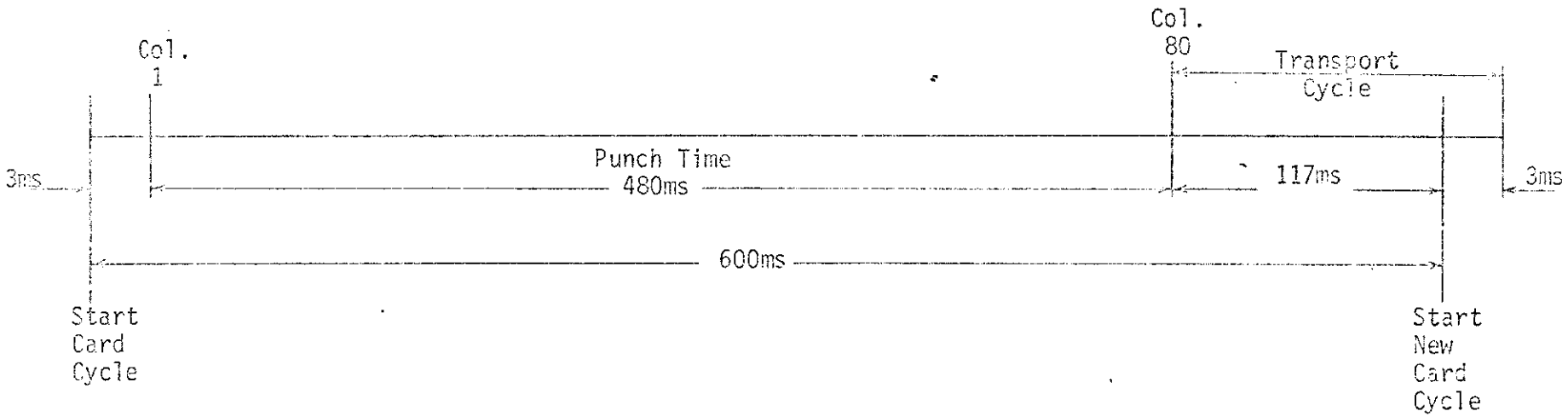
3.1.3.3.6 If the peripheral device is "Ready", and an Invalid Command is not present in the Command register, execution of a Start I/O control function will set the Feed Flip Flop. This FF provides the Feed Command to the peripheral device to begin a new card cycle. A Start I/O control function must be executed for each card. The Feed FF is reset if the Active FF is reset, or upon detection of the trailing edge of the End of Card signal from the peripheral device. For card cycle timing, refer to Figure 3.1.1.

3.1.3.3.7 Control of Inbound Data Transfers is as follows: The peripheral device pulses the Busy line once for each card column as it is read and the column data is stable on the twelve Card Data lines. The Busy line leading edge is detected and used to strobe the data into the Input Data register. This same strobe is used to set the CPU Data Request FF and the Register Full FF. The Register Full FF is reset when the micro-processor reads the Input Data Register, or when it executes a Clear Status control function. Refer to Timing Diagram 3.1.2 for inbound data transfer timing. In the event that the Busy line is pulsed for a new data transfer and the Register Full FF is already set, loading of the Input

500 cpm Read Cycle

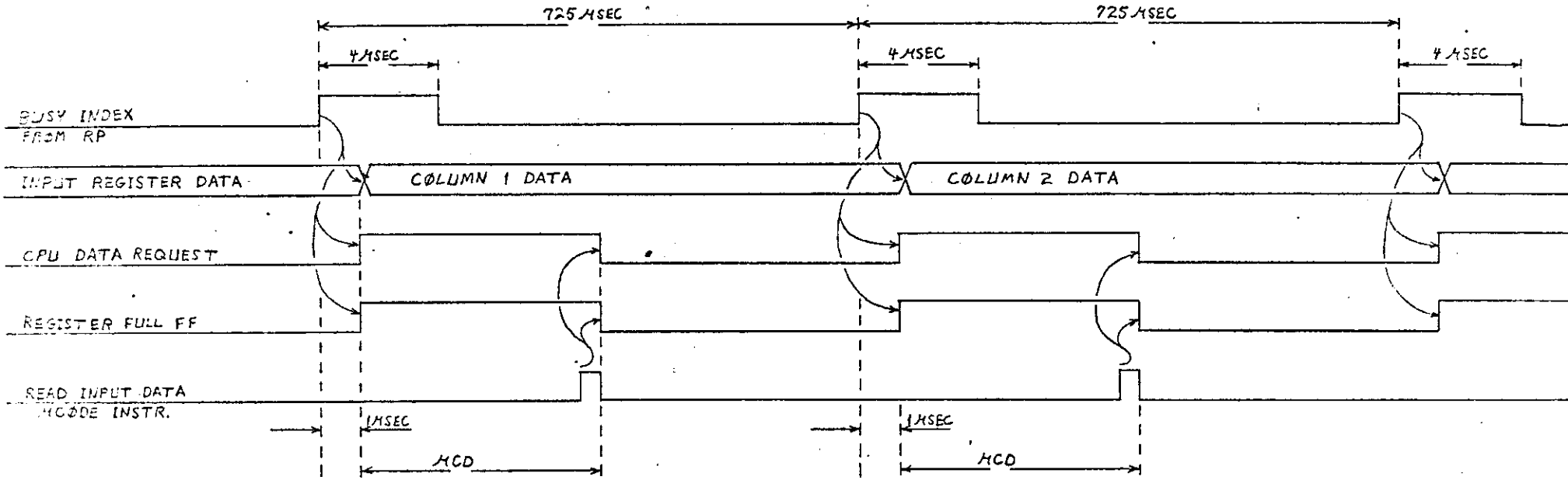


120 cpm Punch Cycle



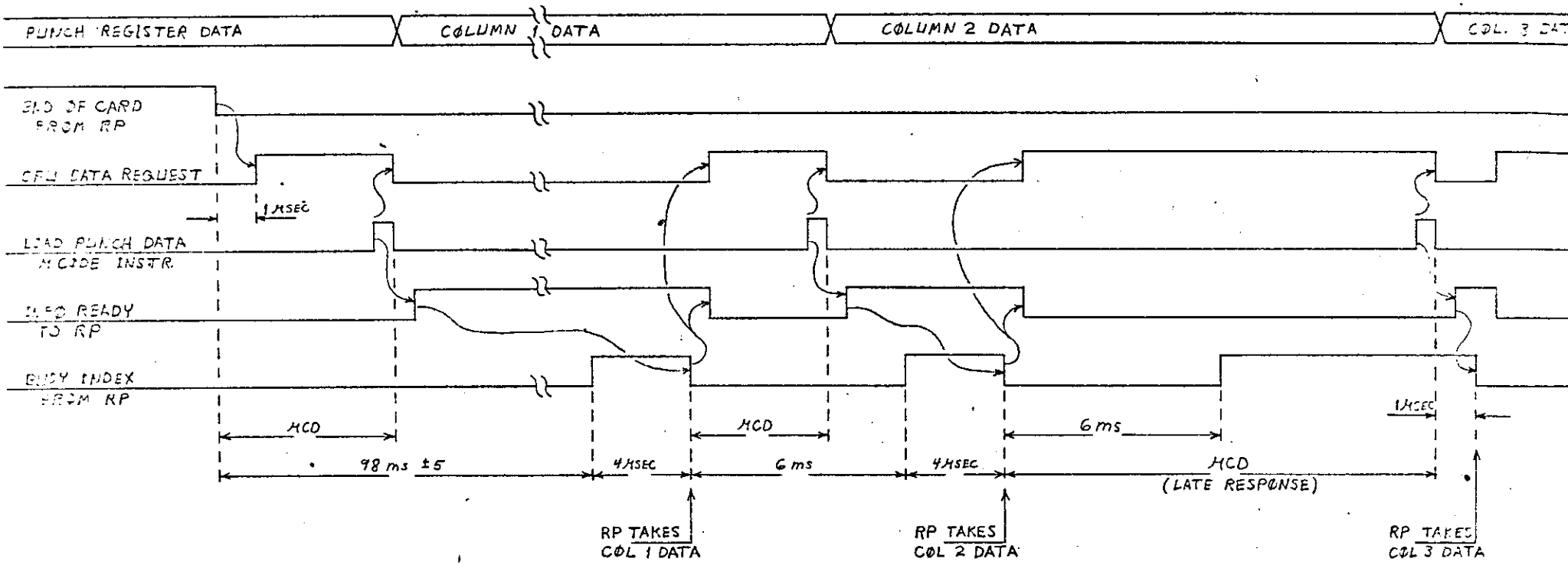
CARD CYCLE TIMING

Figure 3.1.1



NOTE: μCD = MICRO CODE DEPENDENT

TIMING DIAGRAM 3.1.2
INPUT DATA CONTROL TIMING
MRX 80 READER/PUNCH ADAPTER
FOR CONTROL DATA MODEL 9280
(80 COLUMN)
(PRELIMINARY) 6-15-72



NOTE: MCD = MICRO CODE DEPENDENT

TIMING DIAGRAM 3.1.3
OUTPUT DATA CONTROL TIMING
MRX 30 READER/PUNCH ADAPTER
FOR CONTROL DATA MODEL 9220
(80 COLUMN)

(PRELIMINARY) 6-15-72

Data register will be inhibited and the Overrun FF will be set, signaling a data loss error. The Overrun FF can be reset only be execution of a Clear Status control function.

3.1.3.3.8 Control of Outbound Data Transfers is as follows: The peripheral device will set the CPU Data Request FF upon recognition of the trailing edge of the End of Card signal. The micro-processor will respond by loading the first character into the Punch Data register. The Load Punch Data strobe also resets the CPU Data Request FF and sets the Info Ready FF. The Info Ready term signals the peripheral device that Punch Data is available. The peripheral device signals the IRPA80 that it has taken the Punch Data by pulsing the Busy line. The trailing edge of this pulse is detected and is used to reset the Info Ready FF, and to again set the CPU Data Request FF. The micro-processor then responds with new data and the sequence is repeated until all punch data for one card has been transferred. (Refer to Timing Diagram 3.1.3 for outbound data transfer timing.) This data transfer sequence may be terminated earlier than 80 columns, if desired, by execution of a new Start I/O (Feed) control function. Overrun cannot occur on outbound data transfers.

3.1.3.3.9 The Busy FF denotes that a peripheral device card cycle is in process. It is set by the Feed Command and is reset by detection of the End of Card (EOC) leading edge, or upon resetting of the Active FF.

3.1.3.3.10 The peripheral device raises the Ready line if it is on-line and there are no error conditions. The device raises the Status line if it is Ready, the motor is on, and cards are present in the Read Ready and Punch Ready stations. If both of these lines are true, the Ready Latch will be set. If either line is false, the Ready Latch will be reset.

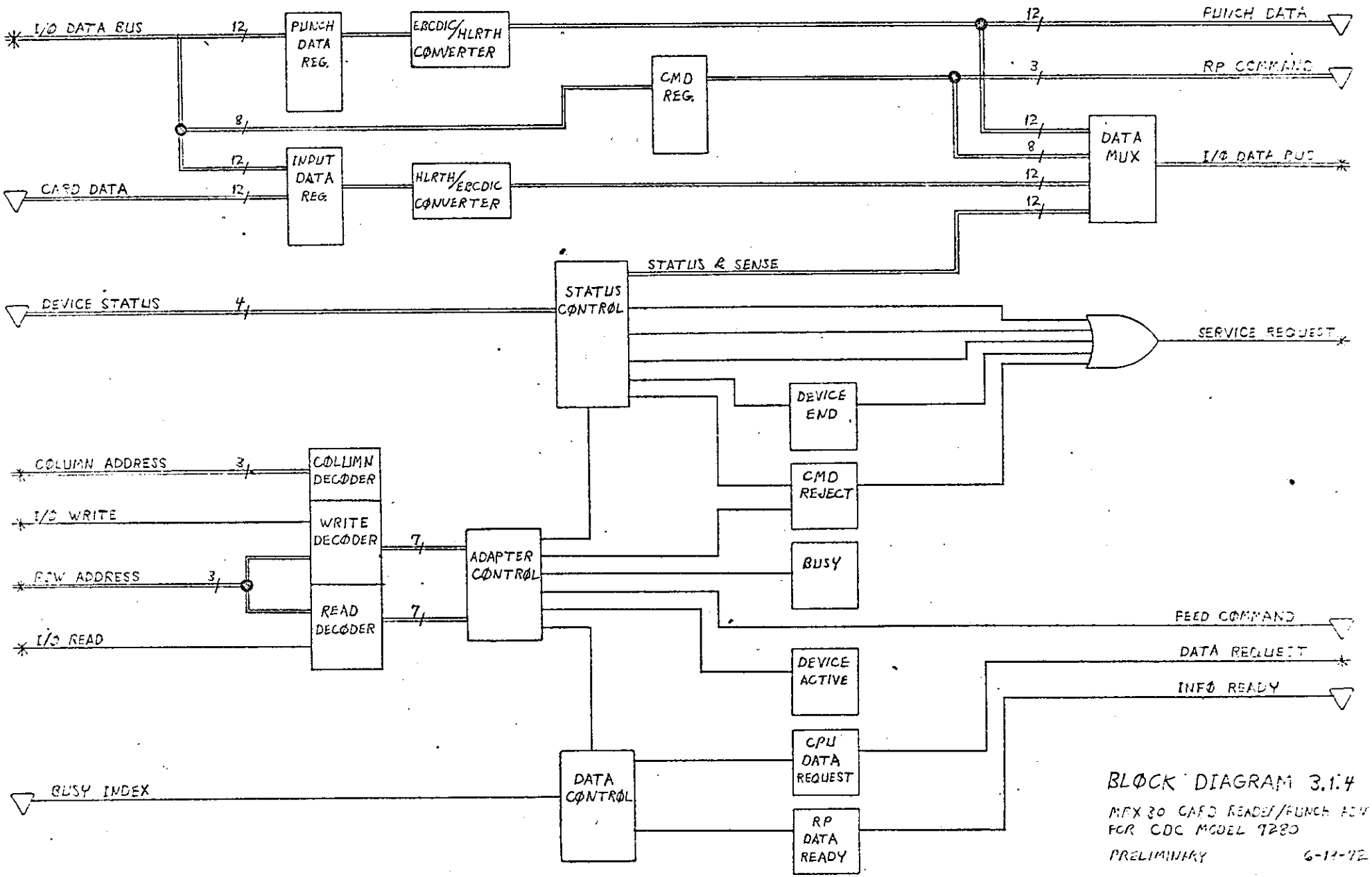
3.1.3.3.11 The leading edge of the Ready Latch is detected and is used to set the Attention FF. The Attention FF is reset by the Clear Status control function. The attention signal raises the Service Request line to signal the micro-processor that the peripheral device is On-line and ready for use.

3.1.3.3.12 The Device End FF is set by the leading edge of the Ready Latch, or by the leading edge of the End of Card signal. It is reset by the Clear Status control function. The Device End signal denotes that the peripheral device has completed its card cycle and is available for a new Feed Command or, in combination with the Attention signal, that the device has come On-Line and is ready for use.

3.1.3.3.13 The peripheral device will pulse the Error Strobe if it detects a "light or dark probe error" during read mode, or if it detects an "echo check error" during punch mode. This Error Strobe line will, if pulsed, set the Data Check FF. If the IRPA80 is not in Binary Image mode this flip flop will also be set by the Hollerith Not Valid signal. The Data Check FF is reset by the Clear Status control function.

3.1.3.3.14 The Command Reject FF will be set by an illegal Read or Write Row address, or if a Start I/O is executed when the peripheral device is not ready, or if a Start I/O is executed when the Command Register contains an invalid command. It is reset by the Clear Status control function. The Command Reject signal inhibits the Feed Command logic and the CPU Data Request logic, and signals the micro-processor that an operational error condition exists.

3.1.3.3.15 The Service Request line provides the IRPA80 with the capability to signal the micro-processor that service is required. This line is raised by setting the Attention FF. Also, if the Active FF is set, this line will be raised by setting of the CPU Data Request FF, Device End FF, Overrun FF, Command Reject FF, Data Check FF, or by the Ready latch being reset.


I/O DATA BUS
12
PUNCH DATA REG.
EBCDIC/HLRTH CONVERTER
CMD REG.
8
12
PUNCH DATA
3
RP COMMAND
12
8
12
DATA MUX
I/O DATA BUS
CARD DATA
12
INPUT DATA REG.
HLRTH/EBCDIC CONVERTER
12
STATUS & SENSE
STATUS CONTROL
DEVICE STATUS
4
SERVICE REQUEST
DEVICE END
CMD REJECT
BUSY
COLUMN ADDRESS
3
COLUMN DECODER
I/O WRITE
WRITE DECODER
7
ADAPTER CONTROL
ROW ADDRESS
3
READ DECODER
7
I/O READ
FEED COMMAND
DATA REQUEST
INFO READY
DEVICE ACTIVE
CPU DATA REQUEST
DATA CONTROL
BUSY INDEX
RP DATA READY
BLOCK DIAGRAM 3.1.4
MFX 30 CARD READER/PUNCH ADAPTER
FOR CDC MODEL 9280
PRELIMINARY
6-12-72

3.2 NINETY SIX COLUMN CARD INTEGRATED READER-PUNCH ADAPTER (IRPA96)

3.2.1 GENERAL

The IRPA96 is the Integrated Adapter/Controller which contains the hardware interface and control logic required to operate the Decision Data Corp. 96 column card equipment. The models which this adapter will control are:

8610 Data Recorder	(DDC 9601)
8611 Data Recorder/Printer	(DDC 9610)
8630 1200 cpm Reader	(DDC 9630)
8633 300 cpm Reader	(DDC 9625)
8643 300/120 cpm Reader/Punch	(DDC 9635)
8653 300/120 cpm Reader/Punch/Printer	(DDC 9645)
8655 500/240 cpm Reader/Punch/Printer	(DDC 9640)
8660 1000/500 cpm MFCU	(DDC 9650)

3.2.2 DEVICE DESCRIPTION

3.2.2.1 The functions, interface, and control of all DDC models are compatible sub-sets of the DDC 9650 MFCU. Therefore, all peripheral equipment references in Section 3.2 will be in respect to this MFCU.

3.2.2.2 The DDC 9650 MFCU is a 96 column Multifunction Card Unit which consists of two input card hoppers, two read stations, two pre-punch wait stations, a collating juncture, one punch station, one print station, six output stackers, and associated mechanical and electronic control. Also, included are three "full card" buffers for the read, punch, and print stations. The MFCU interface signals are DTL/TTL compatible.

3.2.3 IRPA96 DESCRIPTION

3.2.3.1 The Ninety Six Column Integrated Reader-Punch Adapter logic is contained on two plug-in boards. This logic is divided between a "Register" board and a "Control" board. The IRPA96 interfaces to the micro-processor via the I/O micro-bus, the row and column address lines, the read/write control lines, and the service

request line. For additional information on the I/O interface, refer to Section 2.0.

3.2.3.2 IRPA96 Register Board

The Register Board contains the Command Register, Punch Data Register, 96 column/ EBCDIC logic, Read Control and Write Control decoders, and the Data Transfer Control logic.

3.2.3.2.1 The Command Register is 11 bits in length., During the I/O initiation procedure the micro-processor fetches the Command Bytes from the SIO instruction and loads it into this register. The Command is then available to the micro-processor for testing, and, normally, will remain in the Command register for the duration of one I/O operation. The bits in this register correspond to bits 5 thru 15 of the micro-bus and their meanings are: Punch, Read, Print, Print Separate Data, Upper Hopper Select, Inhibit Input Feed, Stacker Mode Control, and stacker select (three lines).

3.2.3.2.2 The Punch Data Register is the outbound data buffer during Card Punch or Print operations. It is 6 bits in length. This register is loaded by the Write Decoder "Load Punch Data" term. The 8 bit EBCDIC character is taken from bits 8 thru 15 of the micro-bus, presented to the "EBCDIC to 96 column format" converter, and the converted 6 bits are strobed into the register. The outputs of this register are connected to the peripheral interface Punch Data lines. This Punch data is also available to the Input Multiplexer, thus providing the capability for diagnostic testing of the outbound data path.

3.2.3.2.3 The peripheral device continuously maintains a character on the Input Data interface lines. Therefore buffering in the Adapter is not required. This data is present at the inputs to the "96 column format to EBCDIC" converter, and the output of this converter is available to the Input Multiplexer.

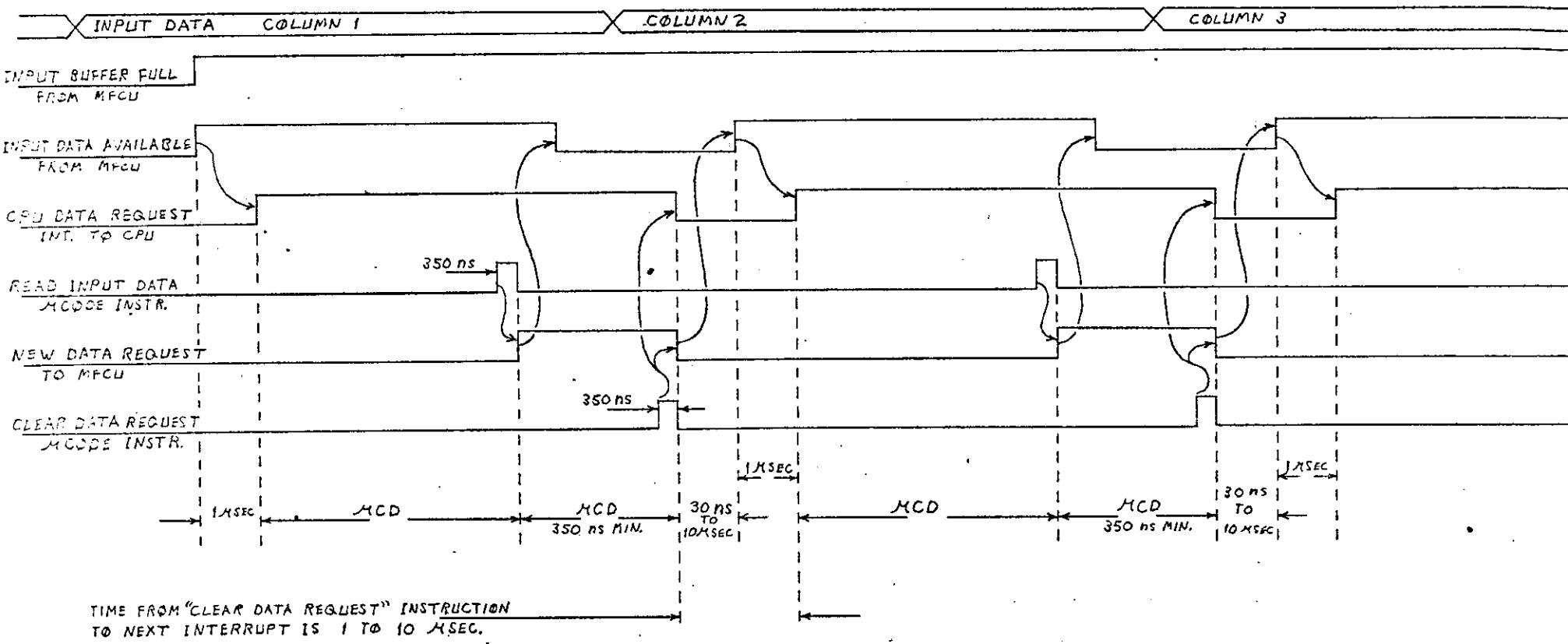
3.2.3.2.4 The Write Decoder is enabled by the I/O write term and, depending on the Row Address contents, decodes one of the following Register Load or Control terms:

1) Load Command Byte (register load)
2) Load Punch Data (register load)
3) Start I/O (control function)
4) Halt I/O (control function)
5) Clear Status (control function)
6) Reset Device (control function)
7) Clear Input Buffer (control function)

3.2.3.2.5 There is one Write address function and one Read address function not used by the IRPA96. These are interpreted as illegal addresses and, should the micro-processor attempt to execute one of these when the Column Address is pointing to the IRPA96, the Command Reject flag will set to indicate an error condition.

3.2.3.2.6 Control of Inbound Data Transfers is as follows: The peripheral device will raise the Input Data Available line for each character, as it becomes available. The leading edge of this signal is detected and the CPU Data Request FF is set to signal the micro-processor that data is available. When the micro-processor executes a Read Input Data micro-instruction, the CPU Data Request FF will reset and the MFCU Data Request FF will set. The MFCU Data Request signal will cause the peripheral device buffer to shift one character and, when the new character is stable, the device will again raise the Input Data Available line. This sequence will continue until all 96 characters are transferred or until the micro-processor executes a Clear Input Buffer control function. Refer to Timing Diagram 3.2.1.

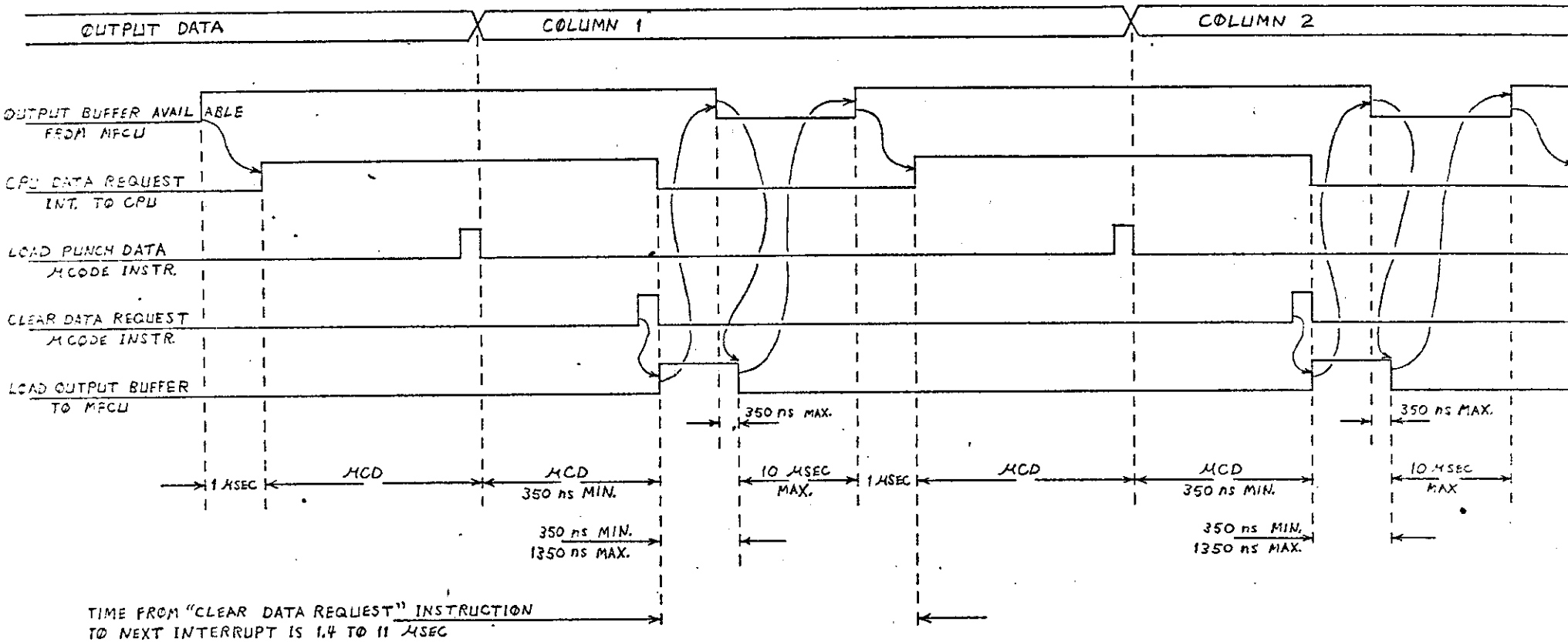
3.2.3.2.7 Control of Outbound Data Transfers is as follows: The peripheral device will raise the Output Buffer Available line as it becomes ready to receive each output character. The leading edge of this signal is detected and used to set the CPU Data Request FF. When the micro-processor responds by loading the Punch register, the Load Output Buffer line will be strobed by the Adapter to signal that data is available. The peripheral device will accept the data and again raise the Output Buffer Available line. This



NOTE: MCD = MICRO CODE DEPENDENT

INPUT DATA CONTROL TIMING

TIMING DIAGRAM 3.2.1
MRX 30 MFCU ADAPTER
PRELIMINARY 5-16-72



NOTE: μCD = MICRO CODE DEPENDENT

OUTPUT DATA CONTROL TIMING

TIMING DIAGRAM 3.2.2
MRX 30 MFCU ADAPTER
PRELIMINARY 5-17-72

sequence will continue until 96 characters have been transferred, or the micro-processor executes a new Start I/O (Feed) control function. Refer to Timing Diagram 3.2.2.

3.2.3.3 IRPA96 Control Board

The IRPA96 Control Board contains the Input Multiplexer, the Data Check logic, Adapter Status logic, and the Peripheral Device Status logic.

3.2.3.3.1 The Input Multiplexer selects the information specified by the I/O Row Address and, if it is a Read operation, the output drivers are enabled, placing the information on the I/O micro-bus. The selected information is one of the following:

1) Input Data (sourced from the input converter)
2) Punch Data (sourced from the output data lines)
3) Command Byte (sourced from the Command register)
4) Status (Attention, Busy, Device End, Unit Check, Request In)
5) Sense 1 (Command Reject, Intervention, Data Check, Not Ready, Upper Input Check, Lower Input Check, Output Check, Stacker full, Lower Hopper Empty, Upper Hopper Empty, CPU Data Request)
6) Sense 2 (Input Data Available, Output Buffer Available, Print Buffer Available, Card In Lower Read Wait Station, Card In Lower Pre-punch Wait Station, Ready for Upper Command, Ready for Lower Command, End of File, Punch Data Check, Read Data Check)

3.2.3.3.2 The Active FF is set if the peripheral device is "Ready" and the micro-processor executes a Start I/O to the IRPA96. It is reset by a Halt I/O. When the Active FF is reset, all service requests are inhibited except "Attention". Also, all data transfers between the IRPA96 and the peripheral device are inhibited. However, all control functions and data transfers between the IRPA96 and the micro-processor are allowed in order to provide for diagnostics, adapter testing, and I/O initiation/termination procedures.

3.2.3.3.3 If the peripheral device is "Ready", execution of a Start I/O will set the Feed FF. This flip flop provides the Feed Request signal to the peripheral device to begin a new card cycle. A Start I/O must be executed for each card. The Feed FF is reset by the Input Buffer Full or Output Buffer Available signals.

3.2.3.3.4 The Busy FF denotes that a peripheral device card cycle is in process. It is set by the Feed Request signal and is reset by a Halt I/O or by the trailing edge of the Ready for Command signal.

3.2.3.3.5 The peripheral device raises the Ready line if it is on-line and there are no error conditions. If this line is true, the Ready Latch will be set. If it is false, the Ready latch will be reset.

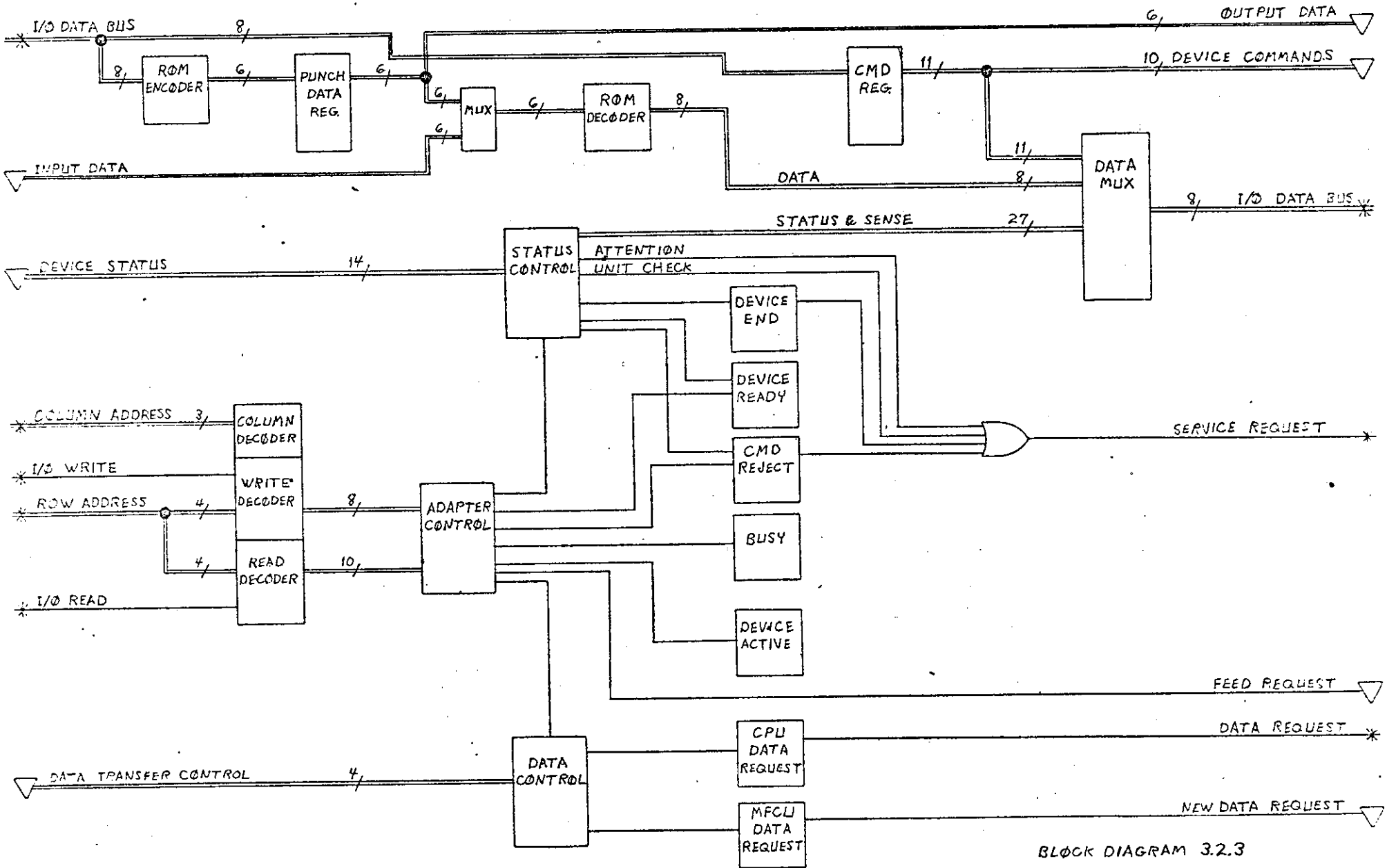
3.2.3.3.6 The leading edge of the Ready latch is detected and is used to set the Attention FF. The Attention FF is reset by the Clear Status control function. The Attention signal raises the Service Request line to signal the micro-processor that the peripheral device is On-Line and ready for use.

3.2.3.3.7 The Device End FF is set by the trailing edge of the Busy signal, or by the leading edge of the Ready latch. It is reset by the Clear Status control function. The Device End signal denotes that the peripheral device has completed its card cycle and is available for a new Feed Command or, in combination with the Attention signal, that the device has come on-line and is ready for use.

3.2.3.3.8 The Data Check signal will go true during a Read operation, if the peripheral device detects a read error. It will go true during a Punch operation, if the peripheral device detects a difference between the punch data and the data read at the Post-Punch Read station.

3.2.3.3.9 The Command Reject FF will be set by an illegal Read or Write Row address. It will also be set by the Start I/O if one or more of the following condtions exist: The Command register contains an illegal command, or upper hopper is selected and the device is not Ready for Upper Command, or upper hopper is not selected and the device is not Ready for Lower Command, or the device is busy, or the device is not ready. The Command Reject FF is reset by the Clear Status control function.

3.2.3.3.10 The Service Request line provides the IRPA96 with the capability to signal the micro-processor that service is required. This line is raised by setting the Attention FF. Also, if the Active FF is set, this line will be raised by setting of the CPU Data Request FF, Device End FF, Command Reject FF, Data Check signal, both hoppers empty, or by the Ready latch being reset.



BLOCK DIAGRAM 3.2.3
MRX 30 MFCU ADAPTER
PRELIMINARY 5-16-72

3.3 INTEGRATED LINE PRINTER ADAPTER (ILPA)

3.3.1 GENERAL

The ILPA is the Integrated Adapter/Controller which contains the hardware interface and control logic required to operate Data Products Models 2440 and 2470 Line Printers.

3.3.2 DEVICE DESCRIPTION

3.3.2.1 The Model 2440/2470 Line Printers contain the electronics and mechanical parts required to print lines of 132 characters on multiple part fanfold paper and advance the paper to the next line to be printed. The control logic required to operate the mechanism electronics and a 132 character buffer register are included. The printing speed (with the standard 64 characters) is 1200 LPM with 68 characters per line, or 670 LPM with the full 132 characters per line. The interface to these printers is DTL/TTL compatible.

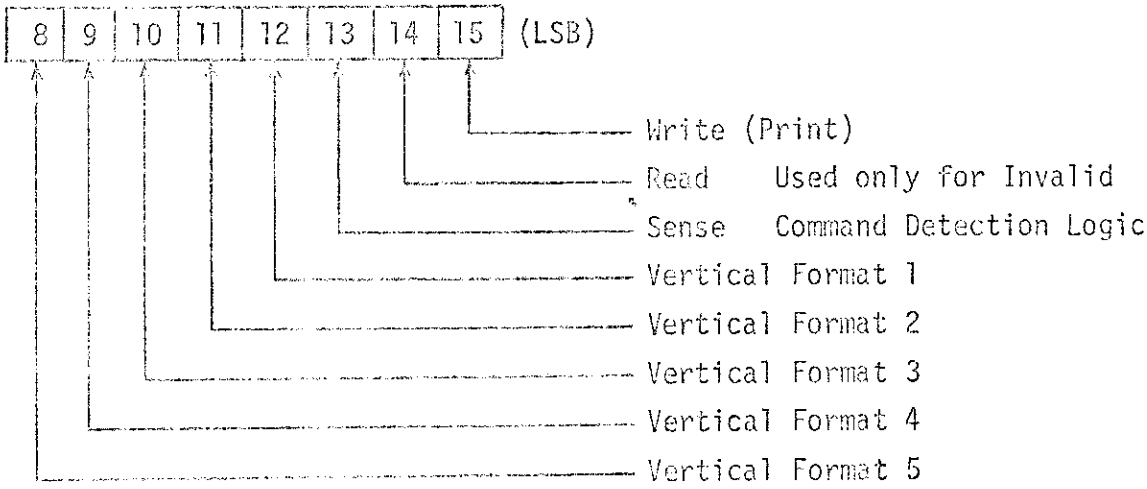
3.3.3 ILPA DESCRIPTION

3.3.3.1 The Integrated Line Printer Adapter logic is contained on two plug-in boards. This logic is divided between a "Register" board and a "Control" board. The ILPA interfaces to the micro-processor via the I/O micro-bus, the row and column address lines, the read/write control lines, and the service request line. For additional information on the I/O interface, refer to Section 2.0

3.3.3.2 ILPA Register Board

The ILPA Register Board contains the Command Register, Invalid Command Detection Logic, Print Data Register, Data Transfer Control Logic, Vertical Format Control Logic, and the Peripheral Device Status Logic. Refer to Logic Diagram ILPA or Block Diagram 3.3.2.

3.3.3.2.1 The Command Register is 8 bits in length. During the I/O initiation procedure, the micro-processor fetches the command byte from the SIO instruction and loads it into this register. The command byte is then available to the micro-processor for testing and, normally, will remain in this register for the duration of one I/O operation. The bits in this register correspond to bits 8 through 15 of the micro-bus and their meanings are assigned as follows:



3.3.3.2.2 Each of the Vertical Format Control Codes required for these line printers is one less, in binary value, than the corresponding codes used in standard software. The vertical format bits from the command register outputs are applied to VF code decrement logic which decrements the binary value, thus correcting this discrepancy. The outpus of this logic are available to the LP Data Multiplexor.

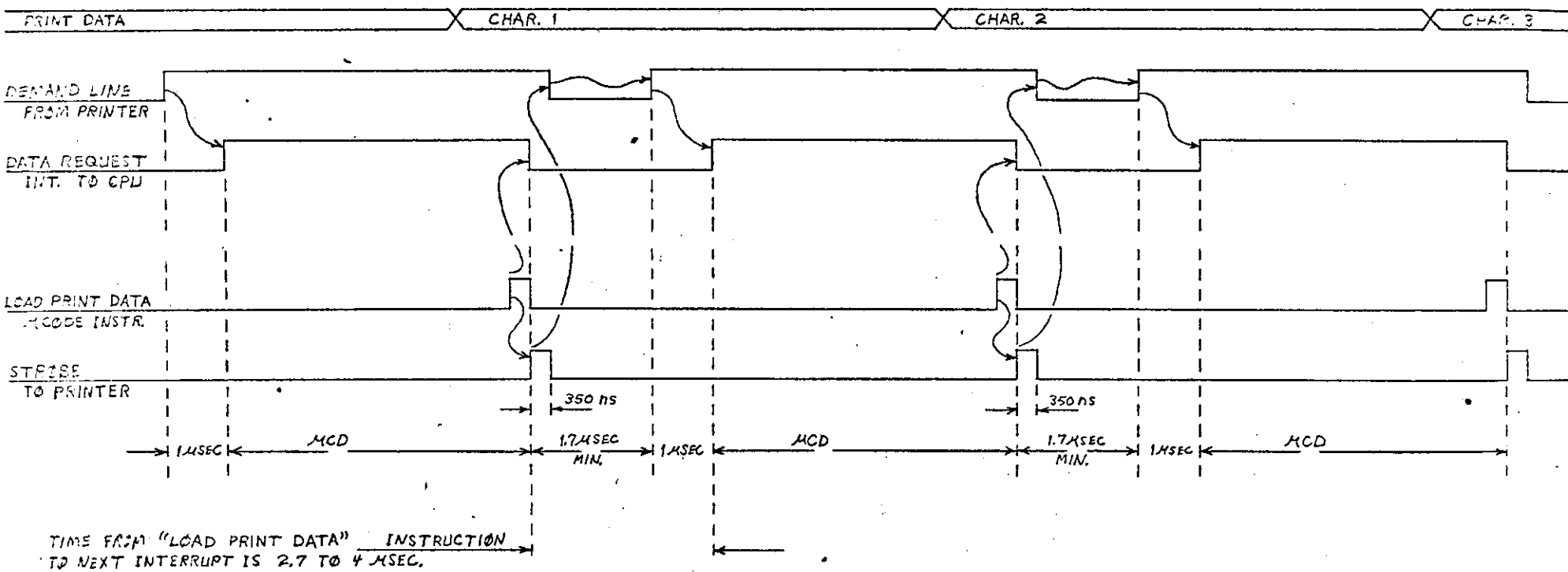
3.3.3.2.3 The Invalid Command Detection logic tests the four least significant bits of the command register. Three of the sixteen possible combinations will be sensed as an invalid command. These are:

1. 0000 Invalid
2. 1000 Transfer in Channel
3. 1100 Read Backward

The invalid command term is one of the inputs to the command reject logic on the control board. However, the invalid command term will not cause a "Command Reject" to occur unless it is present when the micro-processor issues an "Execute Vertical Format" control function.

3.3.3.2.4 The Print Data Register is a single character buffer for the print data. It is 8 bits in length, and they correspond to bits 8 through 15 of the micro-bus. The outputs of this register are multiplexed with the vertical format lines of the command register. The contents of one of the registers is always present on the LP data lines to the peripheral device. This resultant data is also available to the Input Multiplexor, thus providing the capability for diagnostic testing of the data path.

3.3.3.2.5 Control of Data Transfers is as follows. The peripheral device raises the demand line to signal that its buffer is ready for a character. The demand line sets the CPU Data Request FF. The micro-processor will respond by loading a character into the print data register. The load print data strobe resets the CPU Data Request FF and sets the data strobe latch. The



NOTE: MCD = MICRO-CODE DEPENDENT

TIMING DIAGRAM 3.3.1
OUTPUT DATA CONTROL TIMING

MRX 30 LINE PRINTER ADAPTER
DATA PRODUCTS MODELS 2440 & 2470
PRELIMINARY 6-5-72

data strobe signals the peripheral device that the character is on the LP data lines. The device loads the character into its buffer and again raises the demand line. This sequence is repeated until all characters for one printer line have been transferred, or an "Execute Vertical Format" control function is issued. (Refer to Timing Diagram 3.3.1.)

3.3.3.2.6 Vertical Format control of the peripheral device is accomplished as follows. The micro-processor issues an "Execute Vertical Format" control function to the ILPA. This sets the Vertical Format FF which, in turn, switches the LP Multiplexor and raises the Vertical Format Control line. This line signals the peripheral device that the character on the LP Data Lines is a Vertical Format Control character from the command register. The actual character transfer follows the same sequence as that described in Paragraph 3.3.3.2.5. The peripheral device stores the Vertical Format Control character but completes the printing of all data characters previously received, prior to acting upon the control character.

3.3.3.2.7 The Busy signal denotes that the peripheral device is in the process of either printing a line of characters, or moving the paper under Vertical Format Control. The Busy signal is TRUE if the demand latch is set, or the Vertical Format FF is set.

3.3.3.2.8 The Ready latch is set if the peripheral device is "Ready" and "On-line." It is reset if either of these is not true, or if the device detects a forms jam, end of forms, or format tape missing.

3.3.3.2.9 The leading edge of the Ready latch is detected and is used to set the Attention FF. The Attention FF is reset by the clear status control function. The device end signal denotes that the peripheral device has completed its print and paper advance cycle or, in combination with the attention signal, that the device has come on-line and is ready for use.

3.3.3.3 ILPA Control Board

The ILPA Control Board contains the write control decoder, the input multiplexor, and the active and command reject FF's.

3.3.3.3.1 The I/O Row Address is presented to the write decoder and the Input Multiplexor. The Input Multiplexor selects the information specified by the I/O Row Address and, if it is a read operation, the output drives are enabled, placing the information on the I/O micro-bus. The selected information is one of the following:

1.	LP Data	(sourced from the LP Data mux.)
2.	Command Byte	(sourced from the Command Register.)
3.	Status	(Attention, Busy, Device End, Unit Check, Request In)
4.	Sense	(Command Reject, Intervention, Data Check, Not Ready, On-line, Forms Jam, End of Forms, Format Tape Missing, Vertical Format, Demand, CPU Data Request)

3.3.3.3.2 The Write Decoder is enabled by the I/O Write Term and, depending on the row address contents, decodes one of the following register load or control function terms.

1. Load Print Data (register load)
2. Load Command Byte (register load)
3. Start I/O (control function)
4. Halt I/O (control function)
5. Clear Status (control function)
6. Reset Device (control function)
7. Execute Vertical Format (control function)

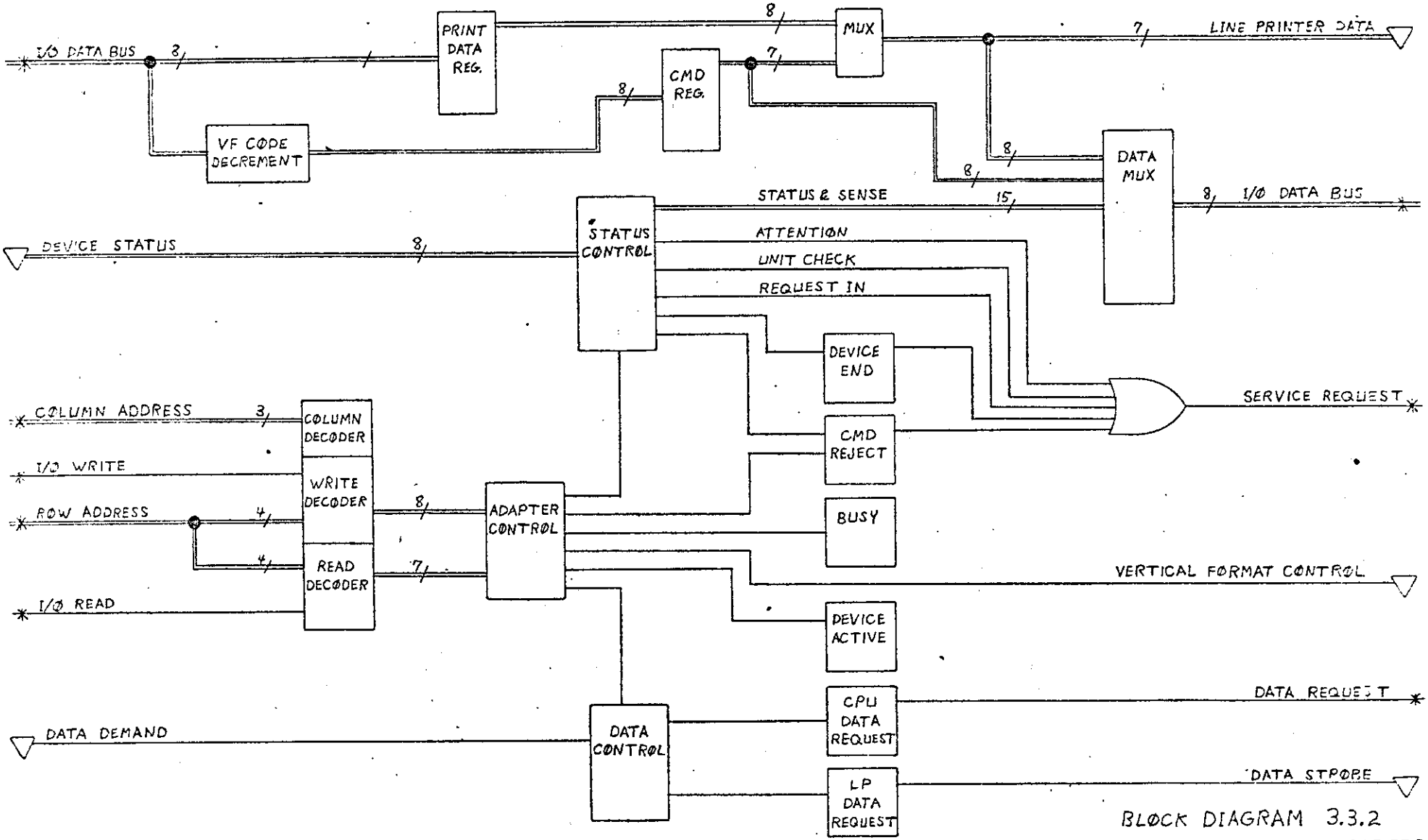
3.3.3.3.3 There is one write address function and four read address functions not used by the ILPA. These are interpreted as illegal addresses and should the micro-processor attempt to execute one of these when the column address is pointing to the ILPA, the command reject flag will be set to indicate an error condition.

3.3.3.3.4 The Active FF is set if the peripheral device is "Ready" and the micro-processor issues a Start I/O control function to the ILPA. It is reset by the Halt I/O control function. When the Active FF is reset, all service requests are inhibited except "Attention." Also, all data transfers between the ILPA and the peripheral device are inhibited. However, all control functions and data transfers between the ILPA and the micro-processor are

allowed in order to provide for diagnostics, adapter testing, and I/O initiation/termination procedures.

3.3.3.3.5 The Command Reject FF will be set by an illegal read or write row address. It will also be set by an "Execute Vertical Format" control function if it occurs when the command register contains an invalid command, or by a "Load Print Data" if this occurs when the peripheral device is either busy or not ready. The Command Reject FF is reset by the clear status control function. The command reject signal inhibits the CPU data request logic, and signals the micro-processor that an operational error condition exists.

3.3.3.3.6 The Service Request line provides the ILPA with the capability to signal the micro-processor that service is required. This line is raised by setting the Attention FF. Also, if the Active FF is set, this line will be raised by setting of the CPU Data Request FF, Device End FF, Command Reject FF or by the ready latch being reset.



BLOCK DIAGRAM 3.3.2

MRX 30 LINE PRINTER ADAPTER
FOR MODELS 2440 & 2470

PRELIMINARY 5-24-72

3.4 CONSOLE ADAPTER

The console adapter provides the interface between the main processor and the console CRT Display Terminal. The console is the means by which the operator can control the operation of the CPU.

3.4.1 DEVICE CONFIGURATION

The adapter will interface with a CRT Terminal at a speed of 9600 BPS or a 1240 Terminal at a speed of 1200 BPS.

3.4.2 THEORY OF OPERATION

The console adapter receives all data and command and transmits data and status from and to the CPU via the I/O micro-bus. The adapter receives characters for the CPU in parallel and disassembles them and sends them serial to the console. The console adapter generates the bit clock for receiving and transmitting 10 bit start/stop characters.

3.4.3 REGISTER USAGE

3.4.3.1 Register Addressing

Address	Read	Write
0	Data	Data
1	Status	Command
2		
3		
4		
5		
6		
7		

3.4.3.2 Data Read

Bit	
0	
1	
2	
3	
4	
5	
6	
7	
8	MS Data Bit
9	
10	
11	
12	
13	
14	
15	LS Data Bit

3.4.3.3 Data Write

Bit	
0	
1	
2	
3	
4	
5	
6	
7	
8	MS Data Bit
9	
10	
11	
12	
13	
14	
15	LS Data Bit

3.4.3.4 Status

0	
1	
2	
3	
4	
5	
6	
7	
8	

3.4.3.4 (Continued)

9 Data Set Ready

10 Carrier Detect

11 Clear to Send

12 VRC Error

13 Stop Bit Error

14 Lost Data

15 Receive Break

3.4.3.5 Command

Bit

0

1

2

3

4

5

6

7

8

9

10

11 Data Terminal Ready

12 Request to Send

13 Write Request

14 Pad

15 Break

3.5 INTEGRATED COMMUNICATIONS ADAPTER

The Integrated Communications Adapter (ICA) is a 16-line multiplexed adapter which transmits and receives information from and to the main processor via the I/O micro-bus. The information flow between the ICA and the terminals is accomplished by leased common-carriers private line facilities, common-carrier switched facilities or equivalent privately owned communications facilities. The ICA is capable of handling any combination of start/stop (asynchronous) lines at speeds up to 1200 BPS, binary synchronous lines (BSC) at speeds up to 9600 BPS and data entry keyboard/display at speeds up to 1200 BPS or one 50KB binary synchronous line.

3.5.1 DEVICE CONFIGURATIONS

The communication terminals that the ICA will support are:

- Memorex 1240/1280 Communication Terminal at speed of 110 BPS, 300 BPS, 150 BPS, 600 BPS, and 1200 BPS.
- IBM 2740 Communication Terminal at 134.5 BPS and 600 BPS.
- IBM 2741 Communication Terminal at a speed of 134.5 BPS.
- Teletypewriter Terminal (Model 33/35/37) at speeds of 110 BPS and 150 BPS.
- Binary synchronous communications terminals at speeds up to 9600 BPS.
- Data entry keyboard at speeds of 110 BPS, 150 BPS, 300 BPS, 600 BPS, and 1200 BPS.

3.5.2 THEORY OF OPERATION

The ICA is divided up into four blocks. They are the control, CRC/LRC/character decode, clock and the line adapter.

The control interfaces with the I/O micro-bus and the line adapters. It also controls the CRC/LRC and character decode. Whenever a line adapter has status or data, a priority flag will be set. This flag is coded by the control to indicate a line adapter address. The control will then set a request for the main processor. The processor will read the address register to determine the line adapter address along with the type of interrupt. Once this is determined the processor will read the data or status register.

When the processor has data or a command for a line adapter, the address is written into the address register, then the data or command is written into the appropriate line adapter. The CRC/LRC/character decode unit accumulates the block check characters or character from the data being sent or received. It also decodes all the data link control characters.

The clock generates all the async bit timing for the LA's.

There are four types of line adapters:

- Asynchronous
- Binary Synchronous
- 50 K B binary synchronous
- Data Entry

All the line adapters have EIA interfaces.

3.5.3 REGISTER USAGE

3.5.3.1 Register Addressing

Address	Read	Write
0	Data/Status	Data/cmd
1	Address	Address
2		
3		
4		
5		
6		
7		

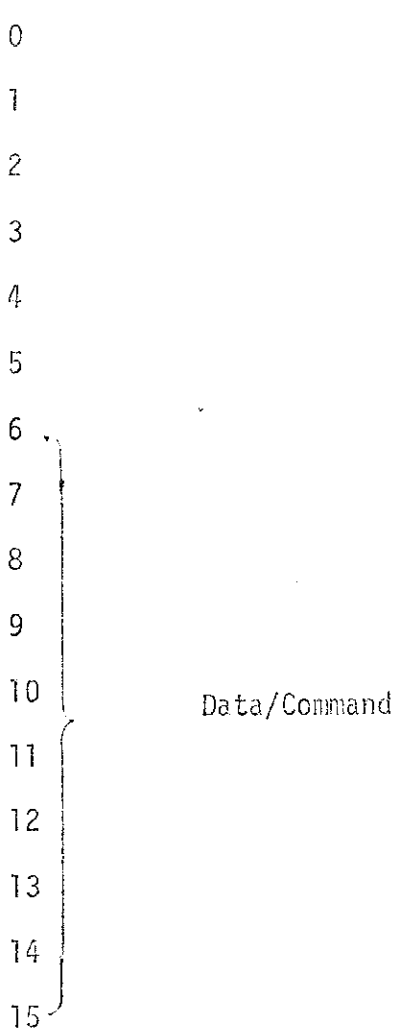
3.5.3.2 Write Address

Bit		
0	cmd = 0	Data = 1
1	cmd 1 = 0	cmd 2 = 1
2	Data Character = 0	Control Character = 1
3	Dial Digit = 1	
4		
5		
6		
7		
8		
9		
10	MS Address Bit	
11		
12		
13		
14		
15	LS Address Bit	

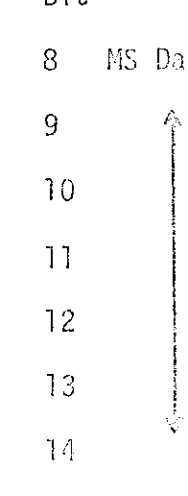
3.5.3.3 Read Address

Bit		
0	Data = 0	Status = 1
1	sol. status = 0	unsol. status = 1
2		
3		
4		
5		
6		
7		
8		
9		
10	MS Address Bit	
11		
12		
13		
14		
15	LS Address Bit	

3.5.3.4 Data/Command Word



3.5.3.4.1 Data Bit Configuration



3.5.3.4.2 Command 1 Bit Configuration

Bit	
1	
2	
3	
4	
5	
6	
7	
8	
9	Data Terminal Ready
10	Request to Send
11	Reset Sync
12	Write Request
13	Call Request
14	Pad
15	Break

3.5.3.4.3 Command 2 Bit Configuration

Bit		
1		
2		
3		
4		
5	EOT Search	
6	Return Unsolicited Status	
7	Return Solicited Status	
8	Clear Link Command	
9	Odd/Error Parity	
10	Parity	
11	MSB	Character Speed
12		
13	LSB	
14	MSB	Character Length
15	LSB	

3.5.3.4.3.1 Character Speed and Character Length

Character Speed		Character Length	
0		0	
1	1200 BPS	1	9 Bits
2	600 BPS	2	10 Bits
3	300 BPS	3	11 Bits
4	150 BPS		
5	134.5 BPS		
6	110 BPS		
7			

3.5.3.5 Data/Status Word

Bit	
0	
1	
2	
3	
4	
5	
6	Data/Status
7	
8	
9	
10	
11	
12	
13	
14	
15	

3.5.3.5.1 Data Bit Configuration

Bit	
8	MS Data Bit
9	
10	
11	
12	
13	
14	
15	LS Data Bit

3.5 .3.5.2 Unsolicited Status Bit Configuration

Bit	
0	
1	
2	
3	
4	
5	
6	
7	Data Set Ready
8	Carrier Detect
9	Clear to Send
10	VRC Error
11	Stop Bit Error
12	Lost Data
13	Ring
14	Abandon Call
15	Receive Break

3.5.3.5.3 Solicited Status Bit Configuration

Bit	
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	Transparent Mode
12	Data Terminal Ready
13	Request to Send
14	EOT Search
15	Synchronization Search

3.6 SELECTOR CHANNEL

The 7100 Selector Channel Adapter is identical to the IBM 360/370 Selector Channel. Transfer rate for data is an excess of 60 K BPS which is accomplished by the direct access to memory. The adaptor design uses the micro sequencer approach. This means that all hand shaking such as raising tag lines, monitoring lines and comparing addresses is achieved by the hardware.

3.6.1 DEVICE CONFIGURATION

The channel can interface with:

a. Line Printers

   1. 5120 Mod 6, 600 LPM Printer
   2. 5120 Mod 12, 1200 LPM Printer

b. Tape Drives

   1. 3237-11 800 BPI, 30 KB Controller Drive, 1 max.
   2. 3237-13 1600 BPI, 60 KB Controller Drive, 1 max.
   3. 3237-21 800 BPI 30 KB Drive, 3 max. w/3237-11
   4. 3237-22 1600 BPI 60 KB Drive, 3 max. w/3237-12

3.6.2 THEORY OF OPERATION

The adapter has a 24 bit micro control word which is used to control tag and data lines and sense for sequencer status, channel status and tag conditions. In order to initiate a sequence the main processor loads the command and address register. If the sequence is a data transfer, the processor will load the memory address register and word count register.

The adapter takes over from there. The next time the main processor gets a request from the selector adapter it will mean either the sequence is complete or it received bad status from the channel or the adapter received a tag or bus error.

The processor will read the status register to identify the status. The micro sequencer consists of 256 words by 24 bits of ROM.

3.6.3 MICRO SEQUENCER WORD

2	2	3	3	5	1	8
TAG	CS	C	PORT	SENSE	R	BRANCH

3.6.3.1 Bus Out

0 NOP

1 Set Hold Out/Select Out

2 Reset Hold Out/Select Out

3 Set Suppress Out

4 Reset Suppress Out

5

6

7

3.6.3.2 Bus On Gating

0 Gate Status to Reg.

1 Gate Address to Reg.

2 Gate Data to Upper DMA Reg.

3 Gate Data to Lower DMA Reg.

4 Set Request Service

5

6

7

3.6.3.3 DMA In

0 Store SRB

1 Gate SRB

2 Decurment Byte Count

3

4

5

6

7

3.6.3.4 DMA Out

0 Date

1 Address

2 Command

3 Gate DMA Data to Bus Out Reg.

4

5

6

7

3.6.3.5 Tag

0 NOP

1 Address Out

2 Command Out

3 Service Out

3.6.3.6 Port

0 NOP

1 Set Operational Out

2 Reset Operational Out

3

4 Read

5 Low Write

6 High Write

7 Full Write

3.6.3.7 Sense

0 Count Complete

1 Tag Error

2 Address Compare

3 Parity Error

4 Status In

5 Address In

6 Service In

7 Suppress Out

8 Chaining

9 Write

10 Operational In

11 Select In

12

13

14

15

16

3.6.4 REGISTER ADDRESSING

	Write	Read
0	Line Address Out	Line Address In
1	Command Memory Load	Status
2	Memory Count Load	Memory Count Read
3	DMA Memory Address	
4		
5		
6		
7		

3.6.4.1 DMA Memory Address

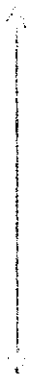
BIT	
0	MS DMA Mem Add
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	LS DMA Mem Add

3.6.4.2 New Count Load/Read

Bit	
0	MS Count Bit
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	LS Count Bit

3.6.4.3 Status Register

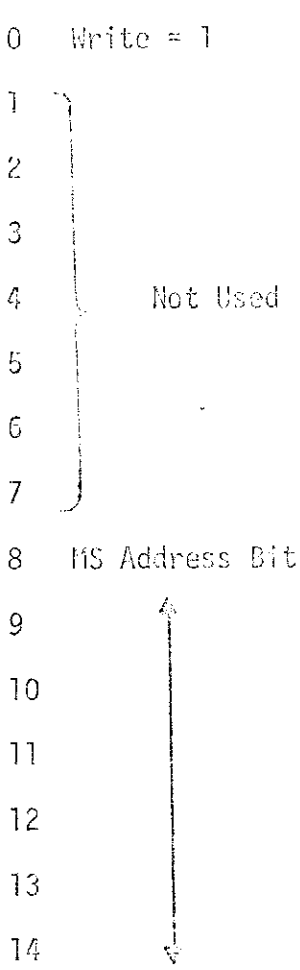
Bit	
0	MS Status Bit
1	
2	
3	
4	
5	
6	
7	LS Status Bit
8	Initial Selection Seq. Error
9	Incorrect Length Transferred
10	Channel Failure
11	Not Used
12	Control Check
13	Transmission Check
14	Invalid Command
15	Not Used



3.6.4.4 Command Register

Bit	
0	Chaining = 1
1	Suppress Length Indicator = 1
2	No Data Transfer = 1
3	
4	
5	
6	
7	
8	MS Command Bit
9	
10	
11	
12	
13	
14	
15	LS Command Bit

3.6.4.5 Line Address Out



3.6.4.6 Line Address In

Bit	
0	Not Used
1	
2	
3	
4	
5	
6	
7	
8	MS Address Bit
9	
10	
11	
12	
13	
14	
15	LS Address Bit