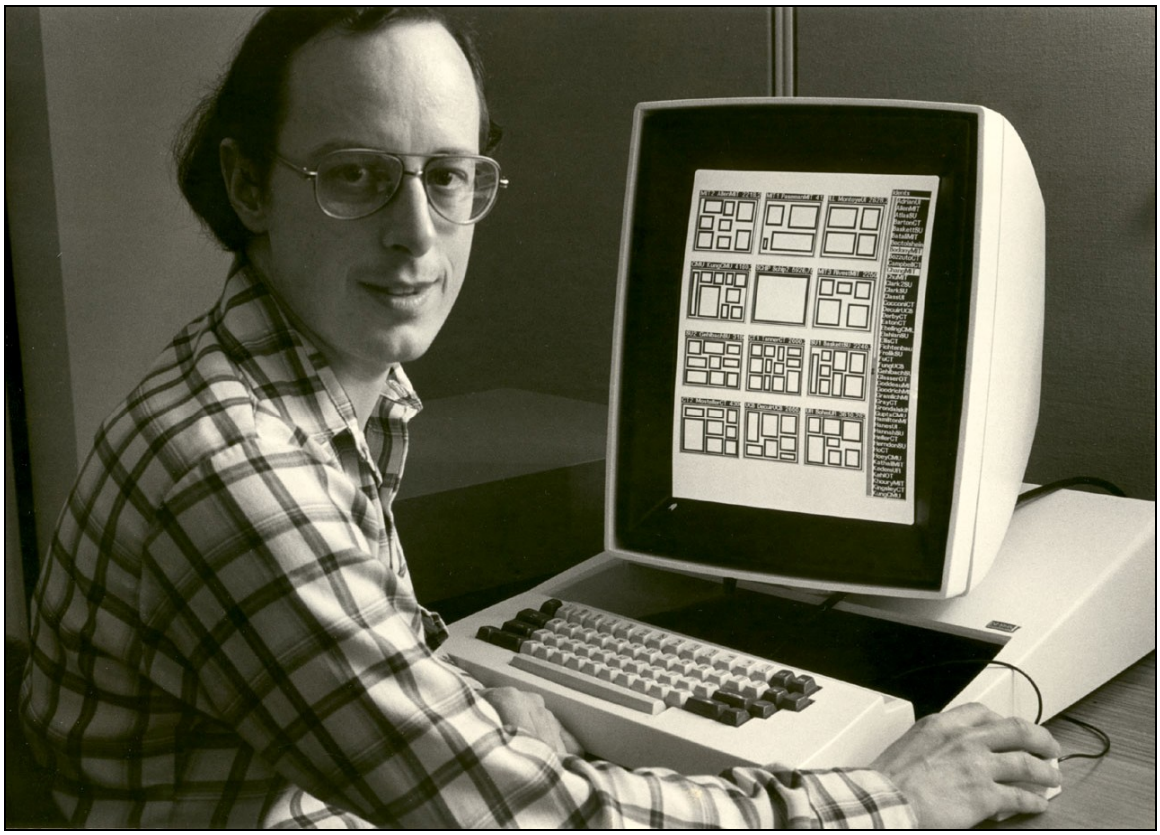
Archive of MPC79 messages, notes and files:

A VLSI Archive Document compiled by Lynn Conway [V 4-08-08].

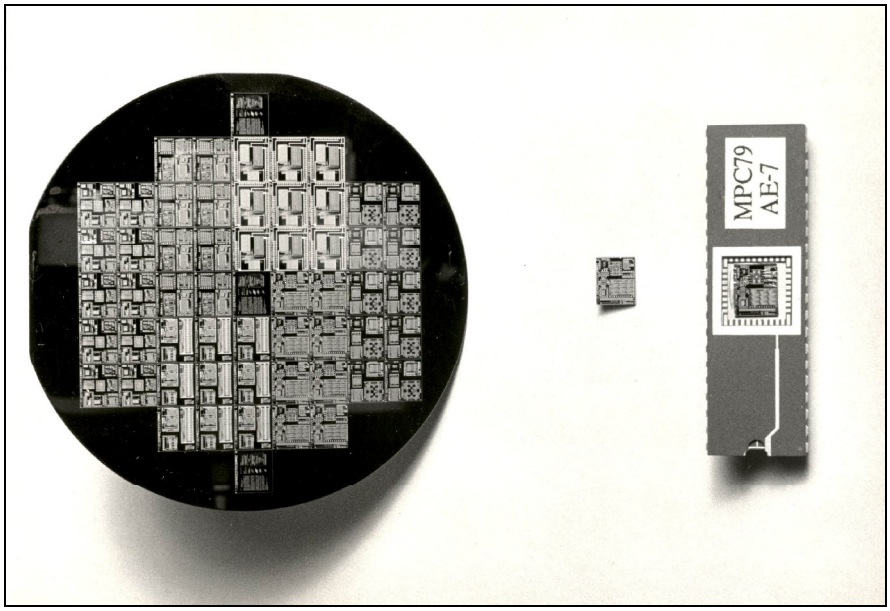
Following the success of her M.I.T '78 VLSI design course, Lynn Conway sought ways to dramatically scale up internet access to quick-turnaround chip prototyping, in order to enable wider testing, refinement and evaluation of the new Mead-Conway design methods. In the spring of 1979 she conceived of a new type of internet-based implementation infrastructure for this purpose, and announced its availability to students taking Mead-Conway courses that fall.

In a crash-effort that summer at PARC, Alan Bell and Martin Newell created a software prototype of the new "MPC System". Lynn's team used the new system to support rapid prototyping of student design projects at many universities that fall, in a large-scale experimental demonstration-trial of the new VLSI design and implementation methods called "MPC79".

MPC79 played a vital role in the rapid evolution and validation of the Mead-Conway design methods and their propagation into over 100 universities and scores of startup companies within just several years. This Archive of MPC79 files contains scans of key documents from that event.



Alan Bell, architect of the prototype MPC software system, overseeing the final merge and die-layout planning of MPC79 projects, Xerox PARC, December 4, 1979.



MPC79 wafer type A, along with packaged and wired-bonded project-chip AE-7, January 2, 1980.

MPC79 Informational Messages:

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
October 12, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **Message #1: Information and Schedules for MPC79**

Filed on: [MAXC] < Conway > MPC79.memo1

GREETINGS!

This is message #1 of a series of messages about the fall 1979 multi-university multiproject chip set (MPC79). A large number of LSI design projects from several universities will be simultaneously implemented in this chip-set. As of now the participating universities are: MIT, Caltech, Stanford, Univ. of Rochester, CMU, and U.C.Berkeley. We may possibly include projects from a few other universities.

This effort has two main purposes: First, it will enable a lot of students and university researchers to have their projects implemented very quickly (we estimate the total turnaround time from design cutoff to packaged chips will be ~4 weeks). Second, it will provide a test of the prototype software and operational procedures we are using to provide this remote-entry, fast-turnaround implementation service.

There are no charges for participation: information management is being provided and maskmaking is being funded by Xerox Corporation; message and design file communication services are being supported by use of the ARPANET; wafer fabrication is being provided by Hewlett-Packard; packaging services will be provided by the universities.

This message provides information about the participating universities and the organizations supplying the implementation service, identifies the design file format, the process, the design rules, and the value of lambda, gives a tentative estimate of the available average space per project, sets certain key dates in the chip-set schedule, lists some tasks to be done by the project lab coordinators, and lists some things to watch for in future messages.

These informational messages are being sent to instructors and project lab coordinators in the universities, and also to those in the ARPA VLSI community who might be interested in following the progress of MPC79. Requests for additions or deletions to the message distribution list, requests for information about MPC79, and all requests for service or status by participants should be communicated by electronic messages via the ARPANET to MPC79@PARC-MAXC.

1. THE PARTICIPATING UNIVERSITIES:

MIT: Course 6.371; Jonathan Allen, instructor; Randy Bryant, TA; 30 students; we estimate that this course will produce 20 projects. We may also include several research prototype designs by MIT faculty members and research staff members.

Caltech: CS/EE181a; Douglas Fairbairn, instructor; Greg Eflan, Dick Lang, TA's; 43 students; estimate 30 projects.

Stanford University: EE292V; Rob Mathews and John Newkirk, instructors; 71 students + 40 auditors; 1st quarter of 2-qtr sequence; most students will complete projects in 2nd qtr; however, we plan to include in MPC79 those students projects completed by the MPC79 cutoff date; we also plan to include some research-prototype designs by Stanford faculty/research staff members; estimate 15 projects.

University of Rochester: EE492/CS492; being taught by a group of EE and CS faculty; Mark Kahrs, TA; 14 students; estimate 10 projects.

Carnegie-Mellon University: Bob Sproull's course is offered in the spring. However, 6 to 8 research prototype designs by CMU faculty members and grad students will be included in MPC79.

U.C.Berkeley: Carlo Sequin's course, CS248, is offered in the winter quarter. However, we plan to include several research-prototype designs by Berkeley faculty members and grad students.

2. ORGANIZATIONS INVOLVED IN IMPLEMENTING MPC79:

Information management for the chip-set will be provided by members of the LSI Systems Area of the Xerox Palo Alto Research Center (PARC), Palo Alto, California. Xerox PARC staff members will (i) support the message and design-file transfer interactions with the university project labs, (ii) provide the technical information necessary for participation, (iii) define the "rules of the game" for space allocation and scheduling, (iv) interact with the various project labs to debug the procedures for interaction well in advance of the final design cutoff date, (v) accept the data files for completed designs, and then (vi) on the cutoff date convert and merge all the designs into mask specifications, and then coordinate maskmaking, wafer fabrication, dicing, and the shipment of wafers/chips back to the universities.

Electronic message service and LSI design file transmissions will be supported by use of the ARPANET. The ARPANET is being used by Xerox PARC and the major universities, all of which are ARPA contractors, to further test the use of such networks for organizing and operating remote-entry, fast-turnaround implemention of large numbers of integrated system designs (an initial feasibility test was made last year in support of the fall '78 MIT course).

Maskmaking for MPC79 will be done by Micro Mask, Inc., Sunnyvale, CA, using an ETEC electron-beam maskmaking system.

Wafer fabrication for MPC79 will be done by Hewlett-Packard at the HP Deer Creek Research Laboratory, Palo Alto, CA, using an nMOS, depletion-load, silicon-gate process.

Packaging: Wafers will be diced at PARC. The chips will be returned to the universities for mounting and custom wire-bonding (we'll send more info about packaging in later messages). Some schools have inadequate wire-bonding facilities, and a limited amount of wire-bonding may possibly be provided by PARC for those schools; we'd like to hear from other schools or firms that could help provide this wire-bonding support.

3. DESIGN FILE FORMAT; PROCESS; DESIGN RULES;
VALUE OF LAMBDA:

DESIGN FILE FORMAT: CIF2.0, as documented in "Introduction to VLSI Systems", by Mead & Conway, Chapter 4; PROCESS: nMOS, depletion-load, silicon-gate process; DESIGN RULES: Mead & Conway (see Ch. 2 and Color Plates 3 and 4 in "Introduction to VLSI Systems"); LAMBDA = 2.5 microns.

4. AVERAGE SPACE PER PROJECT:

Here are some very preliminary estimates: The total number of projects will be ~ 60 to 100. We are planning to produce two E-beam mask sets, with each mask set containing five to seven different multiproject chip types, with each chip being ~ 6mm by 6mm. Thus, the average student project should be ~ 2mm by 2mm. If a university class wants to send some very big projects, they should plan to compensate by sending some small ones to keep the average size down. [We will soon provide a library of cells, including input and output pads that have a pitch of ~106 lambda. Thus at lambda = 2.5 microns, even a 2mm by 2mm project can have ~7 pads on a side, and can contain quite a lot of stuff.]

We are very interested in supporting serious university research projects with these MPC efforts (such as the recent LISP machine chip designed by Sussman, Holloway, Bell, and Steele). Separate consideration for space allocation will be given for such projects.

5. SOME KEY DATES (these are firm deadlines):

(i) Each school should confirm, by no later than 13 November, that the actual software and hardware to be used for final design file transmission to MAXC is operating correctly. This should be done by placing the CIF design file of a typical moderate-sized design on MAXC (the design doesn't need to be in finished form, and doesn't need to be one intended for MPC79, but it should contain a representative collection of CIF primitives and symbols for the purpose of testing the overall system), and then mailing a checkplot of the same file to Lynn Conway, Xerox PARC, 3333 Coyote Hill Road, Palo Alto, CA 94304. We will plot the file here and compare plots to see if the transmission was successful, the CIF code was valid, etc.

(ii) Preliminary "final" versions of all projects must be submitted no later than 27 November. The final space allocation will be made at this time, with those designs earliest to reach the appearance of final form receiving the highest priority. There will be one week remaining to check for errors and resubmit corrected versions before the design cutoff date. However, dimensions of projects may not increase after this time without risk of losing their space allocation.

(iii) The design cutoff date/time will be 4 December at 5:00pm PST. All accepted projects will be gathered at that time and merged into the mask specifications.

6. SOME THINGS TO DO:

(i) Each school should designate some person(s) to be the project coordinator(s). The coordinator

will relay the MPC79 message information, "rules of the game", etc. to those doing design projects at their school, will interact with MPC79 to set-up and test the file-transmissions procedure from their school, and later-on will interact with MPC79 via messages and file transfers to submit design files for inclusion in the chip-set.

(ii) A MAXC account < universityname-VLSI > has been established at PARC for each of the major participating universities to use for MPC79 design file transfers. The project lab coordinator(s) at each university should select a new password for their university's MAXC account, and notify us of that password (we will put it into effect immediately upon receipt). Also, please message the names of the coordinators, and the names of those who will know the MAXC password.

(iii) We will soon begin to make a gross allocation of space between the various schools, so as to provide you all with better estimates of available space. Later-on we'll make firm space allocations to individual projects, with preference given to those projects that are earliest to reach a near-finished form. Coordinators should keep MPC79 updated on the number of projects likely to be submitted by their university. If a school plans to submit several very large designs, let us know as soon as possible, with estimates of the project sizes. If a school expects to submit fewer designs than the estimates listed in item 1 above, please let us know (we can then make the space available to additional participants).

7. THINGS TO WATCH FOR IN COMING MESSAGES:

Message#2 (~ OCT 17): A small library of useful cells and the procedures for obtaining the library design files will be described.

Message#3 (~ OCT 22): The Request-Acknowledge form of interactions will be described for placing design files for checking and for submitting/resubmitting design files for merging into MPC79.

We welcome the students in the courses to the new and rapidly growing community of integrated system designers and researchers. There's a lot virgin territory for you to explore where few have worked before - it's very likely that some of you will discover important new architectural techniques or gain insight into important new research problems while working on your first design projects. We look forward to the excitement of the final month of project activity later this fall. If you have any questions, send us a message.

The MPC79 Organizers,

Lynn Conway, Alan Bell, Martin Newell, Dick Lyon
LSI Systems Area, Xerox PARC
12 October 1979

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
October 17, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #2**

Filed on: [MAXC]<Conway>MPC79.memo2

This is MPC79 message #2, the official release announcement and documentation of the file of library symbol designs provided for use in the multiuniversity multiproject chip set.

SUMMARY

A single file in CIF 2.0 format is provided for your use. It contains standard I/O Pads, all the pieces needed to make PLA's, shift register cells on a pitch compatible with the PLA, and superbuffers for driving clock and control lines. The intention is that these should be a sufficient set of cell designs to allow implementation of combinational functions and state machines simply by placement and interconnection, thus allowing students to focus their efforts on the architecture, logic, and cell designs specific to their own projects. They also serve as examples, and can be used to test your CIF plotting software.

Project lab coordinators at each participating school should retrieve the file from [MAXC]<MPC79>LIBRARY79-250.CIF (250 is the value of lambda in CIF units, which is 2.5 microns). Additional hardcopy documentation with color checkplots will be mailed later to each school.

CONVENTIONS

Since the library symbols were designed using ICARUS, they all have names in addition to numbers. Names are represented in the CIF file by the use of a userExtensionCommand, in the format "9 name;". These names may be used or ignored, but in this message all symbols are referred to by name. The terms symbol and cell are used interchangeably in this message.

In all cases, the origin of a symbol is the upper left corner of its minimum bounding box; hence, all Y coordinates in the CIF library symbol definitions are negative.

Since this library is intended to be compatible with even the simplest design systems, no geometric primitives other than boxes with default direction and no rotation transformations except multiples of 90 degrees are used; all box edges before and after transformation lie on the lambda grid.

Plots of various symbols should be made from the CIF file to serve as the illustrations for this document.

PAD DESCRIPTIONS

Bonding pads and associated circuitry are provided for input, output, clocked output, tristate input/output, Vdd, ground, and conversion of a single-phase clock input to two-phase.

A standard configuration was chosen to simplify placement and interconnection of the pads. See PadBlank, which is called by most of the other pads, as an example:

```
DS 2;          9 PadBlank;
( 4 Items. ); (bounding box 0, 0 to 26500, -26500);
L NM; B L 26500 W 2000 C 13250,-1000; (Vdd line);
L NM; B L 20500 W 2000 C 13250,-25500; (ground line);
L NM; B L 13500 W 13500 C 13250,-13250; (metal pad);
L NG; B L 11500 W 11500 C 13250,-13250; (overglass window);
DF;
```

PadBlank illustrates the fact that each pad is a 135 micron metal square with a 115 micron square overglassing window in a 265 micron (106 lambda) square area, with horizontal metal lines along the top and bottom edges. The top metal line, which is always used for a Vdd connection, crosses the entire width of the symbol, and defines the outside edge of the project of which the symbol is a part. The default orientation is correct for pads along the top edge of a project. The bottom metal line is used for ground, and stops short of the edges of the symbol to facilitate running Vdd around the corners of a project without going outside the bounding box of the pad symbols. A typical project will have abutting pads around two, three, or four sides, with an 8-lambda Vdd ring around the outside, and an 8-lambda ground ring around the inside; pads should only be placed around the perimeter of a project, since interior pads are difficult to bond. The Vdd pad omits the ground line so that there will be a gap in the ground ring to bring power into the project. See PadSample for an example of all the pads and their power connections.

The pads and their sizes (in lambda) are as follows:

PadBlank	106x106
PadGround	106x106
PadVdd	106x80
PadIn	106x106
PadDriver	106x106
PadOut	106x145
PadClockedOut	106x145
PadTriState	106x170
PadClockBar	106x179

The output pads call PadDriver, which uses enhancement-mode pullups, so the output levels are TTL-like; internally these pads should be driven from level-restored signals. The input pad does no level restoration (it simply provides a lightning arrestor), so inputs from TTL-like devices should connect only to k=8 logic, and should not control pass transistors.

Note that PadClockBar generates inverse clocks, guaranteed to never both be low at the same time, from a single-phase TTL-compatible input; these are driven by a powerful superbuffer for distribution around a chip, and are intended to be used with InvertingSB (described below) to generate clocks and gated control signals. Designers should carefully consider the implications of using this clock generation circuit before including it in their projects; it results in considerably less clocking flexibility than using separate input pads for the clock phases.

PLA DESCRIPTIONS

The PLA symbols provided for MPC79 were designed to be simple and clean, and are not as small as they could be in some cases. The pitch of the metal and poly lines in both planes is 8 lambda, when 7 lambda would be possible. This extra spacing makes layout of the edge cells on the same pitch much easier, and makes possible the layout of a shift register cell on the same pitch as the

PLA inputs (16 lambda). The overall structure and orientation of the PLA is similar to that shown in Mead&Conway's Introduction to VLSI Systems, pp. 102-107 (inputs and outputs on the bottom edge, AND-plane on the left, OR-plane on the right); but, as can be seen by comparing the layouts, the extra spacing simplifies most of the cells.

See PLA-4-8-8 (a 4-input, 8-product term, 8-output PLA) as an example of how the pieces fit together. This layout illustrates the use of extra metal ground meshing that may be needed in large PLA's; typically a ground line for every 32 product term lines will be adequate, but a conservative designer might use more frequent ground lines. This layout also illustrates all the possible clocked and unclocked input and output cells, and the NOR ouput cells (which, if used in place of the usual inverters, effectively AND pairs of adjacent OR-plane outputs to facilitate "folding" of ROMs). For simplicity, no provision is made for an odd number of lines across either plane in either direction.

The basic cells provided are the following (cells marked with * should be rotated 90 degrees clockwise for use in the OR-plane):

PlaCell*
PlaGround*
PlaPullups*
PlaConnect
PlaIn
PlaClockedIn
PlaOut
PlaClockedOut
PlaNorOut
PlaClockedNorOut
PlaHoleWires

These are the programming cells for the left and right sides of the AND-plane cells and the top and bottom of the OR-plane cells:

PlaProgLeft
PlaProgRight
PlaProgTop
PlaProgBottom

In addition, cells are provided to fill the spaces left to accomodate the optional extra ground meshing:

PlaOrSpace
PlaConnectSpace
PlaGroundSpace*
PlaPullupSpace*
PlaOutSpace

SUPERBUFFER DESCRIPTIONS

A set of superbuffers is provided for use as clock and control line drivers. They were optimized for flexibility and regularity, rather than absolute speed. SuperBuffer is a subcell of both InvertingSB and NoninvertingSB, and has no output structure of its own. With alternate cells mirrored, superbuffers fit together with their diffusion outputs regularly spaced 16 lambda apart along the top edge. To simplify placement, mirrored pairs are provided for both inverting and noninverting types.

The symbol SBExample illustrates the use of superbuffers with various input options. Generally, it

is intended that Phi1inverse and Phi2inverse from PadClockBar would be distributed on the metal lines that (partially) cross the bottom edge of the superbuffers, and that clock gating signals would be routed in poly from below (low-true logic) into InvertingSB, making it into a NOR driver. Thus both gated and nongated clocks are driven through the same circuit, with similar delay (but use caution in loading these signals, since fatal clock skew is still possible).

The symbol names are as follows:

SuperBuffer
InvertingSB
InvertingSBPair
NoninvertingSB
NoninvertingSBPair
SBExample

SHIFT REGISTER DESCRIPTIONS

These full-bit shift register cells fit together with a pitch of 16 lambda, which make them useful for serial-to-parallel conversion (ShiftCell) on the pitch of PlaIn or PlaClockedIn, or for parallel-to-serial conversion (PSCell) on the pitch of PlaNorOut or PlaClockedNorOut. These cells have vertical metal power and clock lines, parallel to the direction of shift; they should be rotated to interface with the PLA in standard orientation.

The shift register symbol names are as follows:

ShiftCell
PSCell

CHECKING

It is recommended that each designer take the time to examine library cells in detail before using them, to avoid misuse and to look for possible errors or incompatibilities. Although we have checked the cells carefully, they are not guaranteed to be free of logic, circuit, or design rule errors; if any errors are found, please notify MPC79@PARC immediately (the first person to report each fatal error will be amply rewarded). If anyone documents the cells in more detail, such as coordinates of connection points, etc., we would be glad to collect and distribute that information.

It would be useful if instructors would assign homework problems based on the library, such as to look for errors, to analyze the output pad or the clock pad, to develop formulas for the size and speed of the PLA, to analyze capacitive coupling of the clock to the storage node in ShiftCell, or to look at current limits of the power lines in various cells. We would be glad to see the results of such assignments.

Dick Lyon
17 October 1979

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
November 1, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #3**

Filed on: [MAXC]<Conway>MPC79.memo3

This is MPC79 informational message #3, which describes the procedures that project-lab coordinators should use to submit student design files for inclusion in MPC79 and to check the status of submitted designs. We hope the information and examples in this message are sufficient to serve as a "system user's guide" for the coordinators (sorry the msg is so long, but a bunch of examples are included for completeness; future info msgs will be much shorter).

1. OVERVIEW

MPC79 is being used to test some ideas, operational procedures, and prototype software which simulate an automated "VLSI IMPLEMENTATION SYSTEM". Such systems might in the future reside as servers on the ARPAnet or other networks, queuing up requests for implementation of VLSI designs, packing designs into mask sets, generating a mask specification file when a mask set is fully packed, coordinating and tracking the later mask-fab-packaging steps, routing the packaged chips and associated information back to the designers, and then billing the appropriate accounts.

Designer's interactions with such servers could be kept very simple, being analogous to sending electronically created documents to be hardcopied on a centralized printing server in a computer network: when the document (design) is complete, one merely ships the file to the printer (implementation system) and issues the command HARDCOPY (IMPLEMENT); if the document (design) sits in the printer's (implementation system's)input queue for a while, and an error is found in the meantime, one might issue a command to replace the queued entry with a revised entry, etc.

Due to some practical constraints (number of MAXC accounts, security, etc.), we aren't set up to provide all individual designers direct interactions with the MPC79 system. Instead, most designers at each school will have their interactions handled for them by their project-lab coordinators.

Thus the coordinators carry a heavy responsibility for tracking the progress of the student projects, for promptly sending design files and commands to MPC79 as projects near completion, and for keeping the students informed of the status of their designs in MPC79.

However, coordinator interactions with MPC79 should be simple and straightforward, using very simple requests for service via very concise messages; the messages will be easily constructed in response to the usual message system prompting. At most schools, coordinators will simply send a batch of requests every few days, and check on the status of these requests every few days, mainly during the final weeks before the deadlines. We suggest that each coordinator keep in close touch with their student designers via the electronic message system on the computing facilities used for design support at their school.

Here at PARC the MPC79 organizers will initiate responses to coordinator messages, and will

service the requests in those messages, by simply filling in or moving around text entries in "electronic forms" displayed on our ALTOs. In some cases, the message responses and command actions will be automated, but most will require manual keyboard-display interactions on our part. We now expect to receive and process about 60 to 100 projects from about 8 to 10 different schools; thus the need for simple interactions by formal messages.

The following sections describe the types of requests, and give examples to clarify the request message formats and the effects of request servicing by the system.

Some basic ideas and terms used in the following sections are: (i) each project will be given a unique name (ID); (ii) there are only a few request types, encoded by KEYWORDs; (iii) most requests for service need be only one line of text within a message from the coordinator to MPC79@PARC-MAXC of the form: "KEYWORD: ID"; (iv) when the MPC79 system notices and services a request, it will send a message back to the coordinator, indicating a positive (ACK) or negative (NACK) acknowledgement to that request; (v) as nearly-completed designs having valid CIF code and of acceptable sizes are submitted for implementation and ACKed, they will be entered into a PROJECT PENDING QUEUE (PPQ)in order of date/time first ACKed; (vi) space will be firmly allocated to projects in the PPQ in order of entry; (vii) under certain conditions, projects in the PPQ may lose their ACK status - they must regain it by the cutoff date in order to get into MPC79; (viii) a STATUS FILE will be maintained for each school on MAXC showing the current status of that schools projects.

NOTE: Coordinators should keep their MAXC accounts as free as possible of unused files, to avoid excessive use of MAXC file space and to avoid confusion. Think of MAXC as a temporary place for files in transit into MPC79, rather than as a file repository. Just to be safe, we will periodically run a program (DELVER) that deletes old versions of files from the university-VLSI directories, so that only the two most recent versions of any file are retained.

2. THE TYPES OF REQUESTS:

There are five types of requests for service by the MPC79 system that can be made by the university project-lab coordinators: (a) OPEN a project ID; (b) request that an ID's design file be CHECKed; (c) request that an ID's design file be IMPLEMENTed; (d) DELETE a project ID; (e) message an informal QUESTION/COMMENT/ANSWER about a project.

(a) An OPEN causes the MPC79 system to generate a unique ID for a project, and provides the system information for use when responding to messages related to that ID. The OPEN also conveys a brief project description and estimate of project size - this information will be used for setting a preliminary space division in MPC79 among the various universities. (Note: All lengths used for physical space allocation purposes in MPC79 will be given in physical units of microns, rather than in relative units of Lambdas). Once a project is "OPENed", it will be listed in the STATUS FILE. We will begin processing OPENs starting 8 Nov 79. Schools should supply OPENs for projects ASAP after 8 Nov, in order to get an appropriate piece of the available space.

(b) A CHECK request causes a project's design file to be processed by all MPC79 software up to but not including placement in the Project Pending Queue. A project needn't have had space allocated to it to be CHECKed. A CHECK will determine if a project design file was successfully transmitted to MPC79, and confirm that the project's CIF code is OK (to the extent of the MPC79 checking at that time). Requests for CHECKing may occur before a design is ready for IMPLEMENTation. We will begin processing CHECKs on 8 Nov 79. Remember the deadline: each school or other location must have placed a sample CIF design file on MAXC and mailed us a plot of that design by 13 Nov, so we can test the connection to that location. Use a CHECK request for this purpose; the ID can later be closed if the design isn't to be IMPLEMENTed.

(c) An IMPLEMENT request causes a project's design file to be processed by all MPC79 software, to be placed into the Project Pending Queue (if its CIF code is OK), and then to be given a FIRM Bounding Box Space Allocation (if space is available) for merging and implementation in MPC79. Even if the IMPLEMENT is successfully ACKed, the project designer should continue to look for errors (logic, design rule, etc.) in the design. If any are found, they should be fixed; the design file should then be replaced on MAXC, and another IMPLEMENT request issued; this may be done without risk of loss of the design's space allocation, so long as its Bounding Box doesn't increase in size. If the Bounding Box grows, the IMPLEMENT will probably be NACKed, especially late in the game as space is running out. If an IMPLEMENT is NACKed, the designer should be notified by the coordinator ASAP, so that another IMPLEMENT can be attempted. We will begin processing IMPLEMENT requests on 16 Nov 79.

(d) The DELETE request enables removal of an ID from the system by deleting all information from the system related to that ID. Some reasons for a DELETE: A student gets sick, and can't complete their design; a major error in a design is discovered too late to be fixed; the coordinator at a school may want to reallocate space from one big design to several small ones, or vice-versa.

(e) Since the system we're using to conduct MPC79 is an incompletely automated prototype system, and since there's a lot of new and incompletely tested software both here and in the universities, we need an "out" to cover contingencies, disasters, confusions, coordinator or organizer collapse, etc. So, coordinators may request an answer to a QUESTION or send us a COMMENT concerning an ID. We'll ACK these in the usual way (when we're able to get around to them). Similarly, WE may initiate a QUESTION/COMMENT/ANSWER interaction with a project coordinator. However, let's all try to keep this kind of informal interaction to a minimum, and see how far we can get with simple OPEN, CHECK, IMPLEMENT, and DELETE requests.

NOTE: By mid-November we'll process pending requests once every day or two, more frequently as the deadlines draw near. It's possible that multiple requests might be sent regarding one ID before any ACK/NACK is returned by MPC79. In such cases MPC79 will service ONLY the most recent request against the latest file version for that ID.

NOTE: We aren't able to provide users with a "full service". For example, there is no request type "CHECKPLOT" - - -

3. DETAILED DESCRIPTIONS & EXAMPLES OF REQUESTS

NOTE: Please identify requests using keywords followed by colons, as shown below. (In the following, some names & places are real. However, the events are fictitious!).

(a) OPEN:

To OPEN a project ID, the coordinator should send to MPC79@PARC-MAXC a message containing (i) a list of the fullname(s) of the designers of the project, (ii) the person(s) to whom we should send ACKs (usually the coordinator(s)), (iii) persons to copy on the ACKs (perhaps the designers if they have ARPANET mailboxes), (iv) a brief informal description of proposed project (a couple of sentences will do), and (v) a rough estimate of project size (Bounding Box,in microns, for space allocation purposes). Multiple ID OPENs may be requested in a single message; if this is done insert blank lines between the OPENs.

Example of an OPEN request:

- -

Date: 16 Nov 1979 at 0930 EST
To: MPC79@PARC-MAXC
From: REB@MIT-XX
Cc: REB@MIT-XX
Subject: REQUEST

OPEN:
Designer(s): Jim Smith, Jack Jones
ACKs to: REB@MIT-XX
Copies to: SMITH@MIT-AI
Description: This project is a 4-bit slice of an ALU
Est.BB: ~ 1600 X 2600 microns.

OPEN:
Designer(s): Bill White
ACKs to: REB@MIT-XX
Description: Project is a Writeable PLA
Est.BB: ~ 1800 X 2400 microns.

- -

On receiving an OPEN Request, the MPC79 system will (i) establish a "project ID", (ii) file the OPEN information for use when responding to further Requests, (iii) establish and maintain an entry for that ID in the STATUS FILE, and (iv) either Acknowledge the Request by returning the value of the project ID, or Negative Acknowledge the Request with a reason (for example, late in the game we may stop opening ID's). All OPEN REQs will be individually ACKed/NACKed.

Example of an OPEN Acknowledgement:

- -

Date: 16 Nov 1979 at 1820 PST
To: REB@MIT-XX
From: MPC79@PARC-MAXC
Cc: SMITH@MIT-AI
Subject: ACK to OPEN: 16 Nov 1979 at 0930 EST.

Design by Jim Smith, Jack Jones given project ID: SmiJonMIT

- -

(b) CHECK:

To CHECK a design file, the coordinator should (i) place the design file on [MAXC]<universityname-VLSI> using the filename ID.CIF, where ID is the value returned by MPC79 in the ACK to the OPEN for that project, and then (ii) send a message to MPC79@PARC-MAXC requesting "CHECK: ID", as illustrated in the following example. A project needn't have obtained space allocation in MPC79 in order to be CHECKed. For example, the design could be in preliminary form, and be entered for CHECKing in order to test the overall communication link from the university to the MPC79 system, or to test the compatibility of CIF software at both the university and the MPC79 system. Multiple CHECKS may be requested in one message; if this is done, insert blank lines between CHECKs.

Example of a CHECK Request:

```
- - - - - - - - - - - - - - - - - - - - - -
Date: 19 Nov 1979 at 1044 PST
To: MPC79@PARC-MAXC
From: ICL.ISL-ROB@SU-SCORE
Cc: ICL.ISL-ROB@SU-SCORE, ICL.ISL-NUKE@SU-SCORE
Subject: REQUEST

CHECK: RobMSU

CHECK: AndyBSU
- - - - - - - - - - - - - - - - - - - - - -
```

On receiving a CHECK Request, the MPC79 system will pass the design file ID.CIF through all stages of processing up to but not including insertion into the Project Pending Queue, and will either (i) send back an ACK for that ID, which indicates that no errors in the CIF code occurred, or (ii) send back a NACK, indicating an error, along with a brief text comment describing the error. All CHECK REQs will be individually ACKed/NACKed. The time of the CIF file's placement on MAXC and the project's Bounding Box size will be included in the ACK/NACK message.

Example of a NACK to a CHECK Request:

```
- - - - - - - - - - - - - - - - - - - - - -
Date: 20 Nov 1979 at 2018 PST
To: ICL.ISL-ROB@SU-SCORE
From: MPC79@PARC-MAXC
Cc: ICL.ISL-NUKE@SU-SCORE
Subject: NACK to CHECK:RobMSU

NACK to CHECK [MAXC]<SU-VLSI>RobMSU.CIF;1 created 1021/11-19-79.
BB 2200x3200 um.
CIF error: no END statement (did the whole file get to MAXC?)
- - - - - - - - - - - - - - - - - - - - - -
```

(c) IMPLEMENT:

To submit a design file for IMPLEMENTation, the coordinator should (i) place the design file on [MAXC]<universityname-VLSI> using the filename ID.CIF (where ID is the value returned by the MPC79 system in the ACK to the OPEN for that project), and then (ii) send a message to MPC79@PARC-MAXC requesting "IMPLEMENT: ID", as illustrated in the following example. Multiple CHECKs and IMPLEMENTs may be requested in a single message; if this is done, insert blank lines between requests.

Example of an IMPLEMENT Request:

```
- - - - - - - - - - - - - - - - - - - - - -
Date: 23 Nov 1979 at 1845 PST
To: MPC79@PARC-MAXC
From: ICL.ISL-ROB@SU-SCORE
Cc: ICL.ISL-ROB@SU-SCORE, ICL.ISL-NUKE@SU-SCORE
Subject: REQUEST

IMPLEMENT: RobMSU
- - - - - - - - - - - - - - - - - - - - - -
```

On receiving an IMPLEMENT request, the MPC79 system passes the design file ID.CIF through all stages of processing for CHECKing, inserts the design into the Project Pending Queue (if the CIF code is OK) and then allocates space (if space is available). It then either (i) sends back an ACK for that ID, which indicates that no errors in the CIF code occurred AND that space was allocated, or (ii) sends back a NACK along with a brief text comment describing the error or space allocation problem. All IMPLEMENT requests will be individually ACKed/NACKed, with the CIF file's time stamp of placement on MAXC and the BB size included in the message.

Example of an ACK to an IMPLEMENT request:

- -

Date: 24 Nov 1979 at 0700 PST
To: ICL.ISL-ROB@SU-SCORE
From: MPC79@PARC-MAXC
Cc: ICL.ISL-NUKE@SU-SCORE
Subject: ACK to IMPLEMENT:RobMSU

ACK to IMPLEMENT [MAXC]<SU-VLSI>RobMSU.CIF;4 created 1800/11-23-79.
BB 2200x3200 um. Space Allocated.

- -

Example of a NACK to a IMPLEMENT request:

- -

Date: 26 Nov 1979 at 0700 PST
To: ICL.ISL-ROB@SU-SCORE
From: MPC79@PARC-MAXC
Cc: ICL.ISL-NUKE@SU-SCORE
Subject: NACK to IMPLEMENT:RobMSU

NACK to IMPLEMENT [MAXC]<SU-VLSI>RobMSU.CIF;6 created 1340/11-25-79.
CHECKs OK.
BB 2400x3200 um.
BB has grown from previous Allocated BB of 2200x3200 um.
Space not available. Resubmit to Allocated size.

- -

NOTE: We'll be taking a closer look at designs during the final week before 4 DEC, when they are supposedly in near-final form. It is possible that an IMPLEMENT request may receive an ACK from the MPC79 system, and then at a later time our further checking (for example plotting) reveals a fatal error in that design (for example, incorrect layer names throughout a design, gross design rule violations, etc.). If this occurs, the MPC79 system may generate a "Delayed NACK" of that design. So, although the design has achieved a space allocation, it can lose its ACK status at any time, and we reserve the right to do this. The designer must then update the design and the coordinator issue another IMPLEMENT request to try to regain ACK status for the design. The NACK must be replaced by an ACK before the design cutoff date (see item 4).

Example of a Delayed NACK to an IMPLEMENT Request:

- -

Date: 29 Nov 1979 at 2250 PST
To: FOSTER@CMUA
From: MPC79@PARC-MAXC
Cc: HT.KUNG@CMUA
Subject: NACK to IMPLEMENT:MFHTCMU

NACK to IMPLEMENT [MAXC]<CMU-VLSI>MFHTCMU.CIF;3 created 0700/11-25-79.
BB 2800x3000 um. Space Allocated.

Found a fatal error when plotting. Should be easy to fix.
VDD and GND short near logo. Please fix and reissue IMPLEMENT ASAP.
- -

(d) DELETE:

To DELETE an ID, simply send a REQUEST message containing DELETE: followed by the ID. The DELETE will cause deletion of all information related to that ID from the MPC79 system, and will be ACKed by the system when completed. If the reason for the DELETE is a decision to reallocate space to other projects that are on the Project Pending Queue, give the details in the message.

(e) QUESTIONS/COMMENTS/ANSWERS:

If it should become necessary to send a QUESTION or COMMENT, or to ACKnowledge a QUESTION from MPC79 with an ANSWER, use informal messages formatted somewhat like the above.

Example of a QUESTION Request:
- -
Date: 30 Nov 1979 at 1225 CST
To: MPC79@PARC-MAXC
From: FOSTER@CMUA
Cc: HT.KUNG@CMUA
Subject: REQUEST

QUESTION: MFHTCMU: Can't find the error mentioned in your NACK of 29 Nov at 2250.
Have you got a problem with your plotting software?
- -

3. READING THE STATUS OF THE PROJECTS

A file will be maintained for each university on the MPC79 account on MAXC containing the STATUS of that university's projects.

These files will be named [MAXC]<MPC79>universityname.STATUS, where
universityname = "MIT"|"CMU"|"UOFR"|"SU"|"CALTECH"|"UCLA"|"OTHERS".

The project coordinators can read or retrieve these files at any time. For each project ID, the file will contain: the designer name(s); BB in um; AREA in square mm's; if in ACK or NACK STATUS; if project is in the Project Pending Queue; if SPACE is ALLOCATED; the time/date of latest file creation; the time/date of first ACKed IMPLEMENT(sets priority); comments in unformatted text including project decription, open questions, reason for a NACK status, etc.

We suggest that the coordinators retrieve, hardcopy, and post the STATUS file from time-to-time, especially during the final weeks of MPC79, so that students can follow the action.

4. THE COMING SPACE WAR

The above message suggests the space allocation algorithm we'll be using: Basically, it is first-come first-served. While the service is free, participation is somewhat competitive. The PRELIMINARY space partitioning among schools will depend on early OPENs of interesting-sounding projects. (We may modify this partitioning later-on as events unfold). The actual FIRM space allocations among individuals (and the positions in the Project Pending Queue of designs without space allocation) will be prioritized by the first ACKed IMPLEMENT DATEs/TIMEs of individual designs in near final form.

Preliminary final versions of designs (i.e., valid CIF, BB firmly fixed and not to grow, appearance of nearly completed design if plotted) must have been placed by 27 November. Some of these designs may receive space allocations prior to the 27th, but on the 27th we will attempt to make a complete allocation, so that students will know whether or not they are certain to get in the chip set if they finish their designs.

On the design cutoff (5:00pm PST, 4 Dec), all projects having firm space allocation and ACK status will be merged into MPC79; those with firm allocations but in NACK status will be deleted; any remaining space will then be allocated to ACKed projects in the Project Pending Queue, in priority order. We'll send out more messages about space allocation later on as designs are filed on MAXC and we begin to get a feeling for the actual demand vs available space.

Lynn Conway and Alan Bell
LSI Systems Area, Systems Science Laboratory, Xerox PARC
1 November 1979

- -

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
November 6, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #4**

Filed on [MAXC]KConway>MPC79.memo4

This is MPC79 informational message #4, which describes some of the conventions in use for interpreting CIF files. The principal reason for this message is to define the MPC79 interpretation of those aspects of CIF that are influenced by implementation considerations and which typically vary from installation to installation as a function of the plotting and patterning devices to be used.

As was mentioned in Message #1, full CIF 2.0 (as documented in Chapter 4 of "Introduction to VLSI Systems" by Mead and Conway) is being supported by MPC79. Many of the subtle CIF implementation considerations are discussed in Chapter 7 of the upcoming Second Edition of "A Guide to LSI Implementation" by Hon and Sequin (an advance copy of this chapter has been sent to all project coordinators). An overview of some of the more relevant issues is given in this message.

A further motivation for this message is that we can provide better support if certain restrictions are observed. Furthermore, certain constructs take much more processing time than others and we would like you to be aware of these considerations.

1. CIF CONSTRUCTS

This section presents our interpretation of certain CIF constructs.

Box: Straightforward interpretation.

Roundflash: Approximated by an octagon that is always aligned with the overall chip axes.

Wire: For wire segments involving turn angles up to and including 90 degrees the interpretation used is exactly that suggested in Ch. 7 of the Implementation Guide. For sharper angles, no "extension" of the segments is used, but a Roundflash is output at the corner. The ends of wires are always squared off. This interpretation does lead to a sudden change in the shape of a corner as the corner angle passes through 90 degrees, but it was chosen to allow efficient processing of the common case of wires consisting of segments aligned with coordinate axes.

Polygon: All variants of polygons are supported, including non-convex and those with a self intersecting boundary. A point is considered to be inside the polygon if the winding number of the boundary with respect to that point is non-zero. That is, for a point to be considered inside the polygon, a line joining the point to a point moving along the boundary must make a non-zero net number of complete rotations around the given point as the boundary point makes one traversal of the boundary. This interpretation was motivated by the desire for the same results when a self intersecting wire is represented as a CIF wire or as a CIF polygon describing the boundary of the wire. This interpretation is described more fully in Ch. 7 of the Implementation Guide.

User Extension Command: All user extension commands are treated as comments, except that a warning is given.

Layer Names: The following six mask layer names will be recognized and will lead to the inclusion of the affected geometric items into the indicated MEBES mask layer file:

ND Diffusion
NP Polysilicon
NC Contact cut
NM Metal
NI depletion mode Implant
NG overGlass opening

Anything defined on a layer of any other name is treated as unknown, is ignored, and a warning is given. For example, layer NB (Buried contact) is treated as unknown since buried contacts are not supported by MPC79. Layer NX (which is used once in the library sent out) is also in this category.

In general we do not request that the fabrication facility overglass wafers containing multiproject chips. However, overglass masks will be produced for MPC79, and it's possible that some fraction of the MPC79 wafers will be overglassed. Therefore, any bonding or contact pads should have appropriate cuts specified in the overglass layer of the project's CIF file. The Pads in the MPC79 library have such cuts specified, so it will be necessary to specify overglass cuts only if you use some other bonding pads or if you intend to use probe pads.

Delete Definitions (DD): Interpreted as in Ch. 7 of the Implementation Guide. Note that we do not require any DD commands between project files, since in the MPC79 effort we are requiring that projects be self-contained (see also item 3.), so that we can independently process and merge projects into the starting frames.

Warning messages: Our CIF parser produces warning messages on detecting certain questionable constructs (such as zero-width wires, among other things). These may or may not result in the design being NACKed, depending on whether it appears that the error is in fact fatal or not. However, even if the design is ACKed by us, any warning messages should be examined carefully to see if they indicate some serious error.

2. CONSEQUENCES

Roundflash and Wire: In view of the variation in interpretation from installation to installation of the circular arcs found in ideal wires and flashes, it is advisable to adopt a conservative approach to the use of wires. Two extreme approximations to the ideal shapes can be considered - inscribing and circumscribing. If you wish to ensure contact between a wire or flash and some other object in your design (independent of the implementation system to be used) then you should make certain that a system using an inscribing approximation would still place these objects in contact. To ensure adequate separation between a wire or flash and some other object (independent of the implementation system to be used) make certain that a system using a circumscribing approximation would still position these objects with sufficient separation. Whenever the need arises for more precise control over the geometry than can be realized by the above approach then do not use wires or flashes, but use boxes or polygons instead.

The interpretation of Roundflash and Wire commands in MPC79 gives a circumscribing approximation. Consequently there should never be any problem with relying on one of these constructs touching another if that is what is desired. However, design rules may be encroached

upon in some cases where use of the ideal shapes would cause no problems. In particular, consider the corners of the squared off ends of wires, and 90 degree bends.

Polygons: The interpretation of polygons differs from the convention sometimes used in computer graphics of considering that a point is inside a polygon if a line drawn from the point to infinity in any direction intersects the boundary an odd number of times. The interpretation used here is believed to be more relevant to the needs of mask layout. If you are using a different convention, and you have polygons with self-intersecting boundaries, then it will be necessary for you to make adjustments.

3. IMPLEMENTATION ISSUES

CIF Libraries: Each CIF file must provide a complete specification of the design, including copies of any library symbols used. Do NOT assume that we will prefix each project with a copy of the library sent to you. For each project it will be necessary for you to extract, from the libraries provided to you, copies of the symbols used by that project, and to include them in the CIF file for the project.

The impact of your choice of a CIF subset: Various subsets of the full CIF 2.0 may be worth considering for a variety of reasons. It should be remembered that the MPC79 system is experimental, and involves the use of much new and unproven software. Consequently you may hurt yourself, and others, if you set out to push all the facilities to the limits in an attempt to thwart the system. Furthermore, the amount of processing involved in MPC79 will require many hours of computing time here at PARC. Features such as arbitrarily rotated symbols, and contorted wires and polygons can greatly expand the processing time required. Indeed, extreme examples of enormous fully instantiated files that make grossly inefficient use of CIF may find themselves NACKed. You would therefore be doing us (and probably yourselves) a favor if you keep it simple wherever possible.

ICARUS: At several schools the Alto-based system ICARUS is available. A subset of CIF can be converted to and from ICARUS format for viewing or modifying on an Alto. If this is likely to be of interest then the CIF file should contain only Boxes that have rotations of integer multiples of 90 degrees, and Wires having segments aligned with the coordinate axes. Symbol rotations must be constrained to integer multiples of 90 degrees also.

Check Plots: While we are not routinely providing a plotting service, we will be making use of check plots to check on certain designs. Errors found while examining these plots will be reported to you if we believe they represent errors on your part. Consequently, it may be in your interest to make plotting easier for us. At the time of writing this message we have two methods for obtaining check plots, (1) by converting to ICARUS and using its facilities for Versatec and color plots, and (2) by direct plotting of the individual layers on the Versatec only. The first of these gives nice plots but imposes the constraints on CIF cited above. The second is driven off our MEBES conversion software and as such implements everything, however the plots are of single layers only. While we hope to achieve the best of both these worlds in time for use during the later stages of merging MPC79, we cannot be sure of this.

Martin Newell, Alan Bell, Dick Lyon, Bob Hon
LSI Systems Area, Systems Science Laboratory, Xerox PARC
6 November 1979

- -

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
November 26, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #5**

Filed on [MAXC]<Conway>MPC79.memo5

This is MPC79 informational message #5, the final general informational message prior to the design cutoff date. This message (1) discusses some issues related to the open "publication" in MPC79 of design layouts, (2) suggests some basic documentation that designers might include as comments within their CIF code, (3) presents some information concerning the starting frame and packaging, and (4) outlines future messages to be sent and a report to be produced concerning MPC79. Project lab coordinators should pass copies of this message on to the participating designers.

1. THE PUBLICATION OF DESIGN LAYOUTS: SOME ISSUES & OPPORTUNITIES:

The capability for teaching VLSI design courses in the universities and then providing students and university researchers with fast-turnaround implementation of design projects is quite new. Such new technological capabilities often raise novel and unpredicted legal and ethical issues. For example, a question that some designers out there may need to think about is what effect (if any) the open publication of the layout of their design may have on possible proprietary interests they or their organization may have in the design.

The implementation of the MPC79 multiproject chip set is being conducted by the implementing organizations on an open and public basis. There is really no alternative for us since we are using a prototype implementation system, and such things as data security (and also accounting, automated scheduling and planning, etc.) are being deferred to future efforts. The "printing" of the wafers containing the MPC79 projects will be much like the open "publication" of a group of technical articles. We ourselves aren't making any particular efforts to legally register or protect any of the information submitted for inclusion. Our major interest in this effort is to further test the feasibility of large-scale, remote-entry, fast-turnaround implementation of VLSI designs.

There are a number of traditional legal mechanisms for protecting novel designs or works of art (e.g. patents, copyrights, trade-secrets). The inclusion of a design in MPC79 doesn't necessarily preclude use of any of these traditional protections. These can be explored by individual designers (and/or their organizations) on a case-by case basis, as needed. However, do note that the inclusion of a project in MPC79 will result in a release into the public domain of a portion of the information associated with that design, and amounts to a limited form of "publication".

The novelty of this implementation effort will probably generate considerable interest. The various artifacts (plots, chips, chip photographs) associated with MPC79 will get a lot of public exposure. Various portions of these will be reproduced in technical reports and journal papers to be authored by some of the participants (both designers and implementers). It is even reasonable to expect that people at the various schools will examine and analyze available information about designs from other schools, in order to assess the differences in results at the different schools. The design files themselves will exist in several computers including those at the originating university. Thus it is

even possible that some design files could be be released into the public domain, as a function of the data security and the policies at the various intermediate sites they pass through.

O.K., that all sounds like some folks might lose a fraction of their potential proprietary interests in their designs if they include them in MPC79. However, there is another way to look at all this. Because of the large audience that will observe the results of MPC79, any marks placed into the layout itself which identify the design and designer will insure that a large peer group knows who did what. Thus, to whatever extent desired, a designer can obtain recognition in the usual form by obtaining "first publication" via this new medium of "publication".

And so, I suggest that designers at least put their name and/or logo, and perhaps a descriptive design title, right in the layout. If fairly large features on the metal level are used for this purpose, the information will show up well in chip photographs. If this is done, then future plagiarism can at least be recognized. Also, someone wanting to use a design would be able to identify, and then contact and negotiate with the original designer.

There are undoubtedly many interesting underlying issues lurking here that members of the technical community might discuss further with colleagues in law schools, business schools, and public policy groups. Perhaps a fundamental question is what legal and cultural traditions would best strike a balance between providing rewards and protection to the creative designer while at the same time stimulating research and innovation through the free exchange of ideas.

2. DOCUMENTATION OF DESIGNS: SOME SUGGESTIONS:

Because of the wide exposure of MPC79 artifacts, there will likely be requests for further information about particular designs or designers. For example, a company may wish to know how to contact the person who designed project X, in order to inquire about their availability for employment or consulting. We plan to list a moderate amount of basic information (such as designer names, schools, organizations, and project titles, as available) in our future technical reports on MPC79.

Those designers who are interested in receiving this sort of exposure should send some basic documentation along with their design files. A good way for designers to send this information is to insert it as CIF comments right at the beginning of their design files. I suggest that designer(s) include their name(s), school and department address, company name and address if they also work in industry, a short abstract describing their design, and pointers to any available or planned documentation or reports concerning the project.

3. STARTING FRAME AND PACKAGING INFORMATION:

The layout of the starting frame for MPC79 has been completed. There will be only one die size: 7696 X 6477 microns (~ 303 X 255 mils). This is the size as measured from scribe line center to scribe line center, prior to sawing up the wafers. The largest metal-line bounding-box that can be contained within the starting frame is 7548 X 5960 microns. The individual die sizes after sawing will be ~303 X 255 mils plus or minus a couple of mils, depending on how each die fractures below the saw cuts around its periphery (sorry about the English units, but the packaging industry still lives in the past and specs everything in mils). We recommend using standard 40 pins packages with cavity sizes of no smaller than 310 by 310 mils. (Use of larger cavity sizes, for example 340 X 340 mils, might be better since wire-bonding the pads near the edges of the chips would be made easier).

We have access to limited packaging capabilities, and a modest supply of 310 X 310 mil cavity 40

pin packages. We'll likely be able to do the packaging and wire-bonding for a few of the smaller isolated design groups that don't have any access to packaging equipment. We'd appreciate hearing from all the project lab coordinators so that we can learn of your school's capabilities and plans (or lack thereof) for doing the packaging of your MPC79 project chips. If you are planning to do your own packaging, you should either have packages in stock or be able to scrounge them from some local company, or else you should order them instantly in order to have them on hand in time when the wafers are ready. If you have access to local industrial help for packaging, and are able to arrange for some of the other schools to have chips packaged, let us know. Especially let us know if you plan to count on us to do your packaging.

The starting frame surrounding every die type will contain several test patterns having pads that can be be probed or wire-bonded that can be used to confirm that the process worked successfully and also to measure performance and certain electrical parameters. Included are four discrete devices (all having channels 5 microns long and 10 microns wide): (i) an enhancement mode FET, (ii) a depletion mode FET, (iii) a metal-gate field-oxide FET, and (iv) a poly-gate field-oxide FET. A ring-oscillator is included that can be used to measure the transit-time of minimum-sized devices. Also included are two Van der Pauw 4-point resistance measuring structures, to enable measurement of the resistances of specific poly and diffusion paths.

4. FUTURE MESSAGES & REPORTS ON MPC79:

Various announcement messages and messages to specific coordinators or designers will be sent out as needed between now and 4 December. Project lab coordinators should watch their mailboxes closely, especially during the final days before the design cutoff. Note: If project coordinators are ever unable to contact MAXC over the net, don't panic, but try again an hour or so later. In the unlikely event that MAXC goes down for more than on hour (especially if some time during the crunch of the last few days before the design cutoff), we will send out advisory messages to all coordinators via other HOST machines on the ARPANET.

After 4 December we will periodically send out status messages to help you track the progress of the maskmaking and wafer fabrication and to help you plan for the arrival of your wafers/chips.

During January and early February we will be seeking information from those participants who have by then tested their projects. We will be accumulating information about the results of the projects at the various schools, and will send out messages sometime in February summarizing this information.

During January and early February we will be documenting the results of MPC79 for inclusion as part of a Xerox PARC/SSL Technical Report by L.Conway, A.Bell, and M.Newell entitled something like "The Implementation of VLSI Systems". This report will likely be available by April '80. (If you'd like to receive a copy of this report, send a msg to Doughty@PARC-MAXC).

Well folks, were now entering the final week before the design cutoff. Good luck on finishing your projects! Watch your electronic mail to find how it all finally turns out.

Lynn Conway
LSI Systems Area, Systems Science Laboratory, Xerox PARC
26 November 1979
- -

Date ?

Well folks, we're nearing the final design cutoff time! We want to congratulate the many project coordinators and designers out there who have managed to keep up with the demanding schedules and deadlines of MPC79. So far we have about 70 designs likely to make it into MPC79.

The available space is fully allocated. A number of projects previously in ACK status with Space Allocation have since increased in size. These will lose their firm Space Allocation, but will remain on the Project Pending Queue, awaiting allocation (most of these will likely make it). We can't be sure how it will finally turn out, since a lot depends on the packing density effectiveness of our planning software, as run on this specific set of projects.

Since there are a number of projects awaiting allocation, it would be a great help if project lab coordinators would notify us ASAP if there are any projects in ACK status that they know will not be finished in time. Such projects should be DELETEd so that others will have a chance to be included. Even if there are no other designs pending from your school, such DELETions may make space available to someone from another school.

We will attempt to group projects together by school onto the different die types. This will make the later distribution of chips, and the distribution of chip-photos, etc., more efficient. One thing for instructors and lab coordinators to consider: If a bunch of your projects are in a visibly unfinished state, they will greatly detract from the effectiveness of your school's chip-photos, etc. We are not looking at plots of all projects to see if they appear completely finished. We guarantee only that the design files will successfully pass through our processing software. (Even if we could plot all the projects, which we can't due to the plotting time involved, there would be difficult questions of interpretation). So, we ask you coordinators to please pass a final filter over your school's designs (perhaps ask to look at a plot of any designs that are late in nearing completion), and Request a DELETE of any that are unfinished.

[A suggestion: It would be a good idea for coordinators to get a list of the names, addresses, and phone numbers of the participating designers, so that you can contact them (probably in early January) when the chips are ready. We will prepare various reports, make up some chips photos, etc., which you or we could also distribute to the participants, if we have all the names and addresses.]

Remember, the deadline is Tuesday, 4 December, at 5:00pm PST. At that time we will stop processing Requests, and will run the Planning, Packing, Merging, and MEBES Conversion software against the collection of projects in ACK status, pulling in as many projects pending allocation as possible.

We would appreciate it if at least one coordinator or instructor from each school would remain available for last-minute questions or decisions. We will be doing quite a bit of plotting once we have merged groups of projects into starting frames. We might, for example, spot what appears to be a fatal flaw in a design at

that point. If we can reach you for information, you can help us make a decision on whether to dump the project or not.

Since these interactions will be few, but must be quite interactive, we suggest that you message us the name and phone number of the coordinator or instructor for your school who could be reached by phone between the hours of 5:00pm and 8:00pm PST (8:00pm and 11:00pm EST) tomorrow. By 8:00pm PST all the hard decisions will have been made.

We will send out a message later this week, summarizing the final status of the MPC79 merging, indicating which designs actually made it into the chip set, etc.

Lynn Conway, Alan Bell, Martin Newell

Reb
Joy
MF40
Doug
Carlo
Izzy
[illegible]
ROS
NUNC
Forest
[illegible]
MPC79
N. bus
Sur
AB
Conway

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, CA 94304
December 5, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **The Implementation of MPC79 is Underway!**

Greetings!

At 5:00 pm PST Yesterday, we processed all pending Requests, and then collected and merged as many of the remaining ACKed design files as possible into MPC79 (many designs from the project pending queue were included).

A total of 82 designs, created by 124 designers, were included in MPC79. These have been distributed over 12 different die types which will be fabricated in 2 different wafer types.

We ran Alan Bell's and Martin Newell's MPC planning, merging, and format conversion system last night, and successfully processed the entire set of designs. MEBES tapes have been generated for the full chip set. The tapes have been dispatched to Micro Mask, and maskmaking will soon get underway.

Prior to releasing the tapes for maskmaking, we made metal layer plots of all chip types from the MEBES files, as a final check that all was well. A check of these plots indicates that a high percentage of the designs included in MPC79 are in very good shape (as you might expect, there are a few notable exceptions!).

We will keep you informed of the estimated date of availability of the chips as we begin to get feedback from maskmaking and wafer fabrication. We now guess that the first week in January is the most likely time.

We're sure that many students and project lab coordinators out there are anxiously awaiting news about which designs made it into the chip set. There are a few students who are going to be disappointed. Later-on we will provide more feedback to the project lab coordinators so that students can find out why particular designs did or did not make it into MPC79 (we are a bit tired now, and probably won't be on the net for a few days).

However, there are very many students who will be pleased to learn that their designs are included. The following list gives the number of projects, number of designers, and the CIF design file names (append .CIF) by university, of all designs included in MPC79:

MPC79 DESIGN LIST:

MIT: 15 Projects, 27 designers

AllenMIT, BataliMIT, ChuMIT, FichtenbaumMIT, GoddeauMIT, GoodrichMIT, GramlichMIT, GrondalskiMIT, HamiltonMIT, KathailMIT, KhouryMIT, PasemanMIT, PicardMIT, RivestMIT, Schip2(Scheme machine).

Caltech: 24 projects, 28 designers

BartonCT, BozzutoCT, CambellCT, CocconiCT, DerbyCT, EatonCT, EllisCT, FuCT, GrayCT, HellerCT, HoCT, KingsleyCT, LiCT, LigockiCT, MostellerCT, PapachCT, PedersenCT, PinesCT, PursifullCT, RumphCT, TannerCT, WalpCT, WatteyneCT, WhitneyCT.

Stanford: 19 projects, 35 designers

AtlasSU, BaskettSU, BechtolsheimSU, Clark2SU, ClarkSU, ElahianSU, FrolikSU, GehlbachSU, HannahSU, HerndonSU, MacomberSU, MarkeeSU, MathewsSU, NoiceSU, OhChinSU, TarsiSU, UttSU, WulffSU, ZarghanSU.

CMU: 5 projects, 6 designers

EbelingCMU, GuptaCMU, HoeyCMU, KungCMU, SongCMU.

U. of Illinois: 5 projects, 8+ designers

AdrianUI, ClassUI, HanesUI, LuhukayUI, MontoyeUI.

U.C.Berkeley: 4 projects, 4 designers

DecuirUCB, FungUCB, LandmanUCB, SequinUCB.

U. of Rochester: 5 projects, 9 designers

KedemUR, LyonsUR, SohmUR, TiloveUR, WatanabeUR.

OTHERS: 5 projects, 7 designers

GlasserOT, KehlOT, MurrayOT, RodgersOT, SnyderOT.

From the MPC79 Organizers

Lynn Conway, Alan Bell, Martin Newell, Dick Lyon
5 December 1979

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, California 94304
January 5, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #6**

Filed on [MAXC]<Conway>MPC79.memo6

The MPC79 implementation has been successfully completed! The chip-set includes 82 VLSI design projects from 124 designers. The implementation turnaround time for MPC79 was 29 days. (from design files to distribution of packaged chips).

Packages containing the project chips were distributed on January 2, 1980. On January 2 the packages were hand delivered to Caltech, Stanford, and U.C.Berkeley, and were mailed special delivery to instructors or coordinators at M.I.T., CMU, Univ. of Rochester, Univ. of Illinois, and the Univ. of Washington. Packages were mailed to individual designers at Univ. of Colorado and Univ. of Bristol the following day. All coordinators should have received the shipments by now. It's likely that most of the chips will be distributed to the student designers during the next few days, just as the new semester begins at most of the schools.

This message (i) provides information about the implementation activities during the past 4 weeks, (ii) describes what the MPC79 shipments contain, and (iii) describes some things that coordinators should do before distributing the chips and their documentation. It also discusses our plans for further documentation concerning MPC79, and our interest in receiving feedback from the designers, to include in that documentation.

If you have any questions or wish to provide testing results or other feedback, you can continue to reach us via MSGs to MPC79@PARC-MAXC.

THE EVENTS SINCE DECEMBER 4:

The events of the past four weeks since the design cutoff time of 5:00pm Tuesday December 4 have been as follows:

We started final processing of the implementation REQUESTs immediately following the design cutoff time. This processing continued on into the evening. During the night of 4-5 December we operated the MPC implementation system to plan and effect the merging of the projects into the various MPC79 chip-types, and to then convert the merged CIF files into MEBES format files. At 10:00 am the next morning we took the merged mask-specification data to Micro Mask.

Delivery of the masks was pipelined with the early fabrication steps, with the first mask of both mask sets being delivered at 5:00 pm, Thursday Dec. 6. By then, HP-ICPL had already started the

processing and were ready for the first masks. Processing continued normally except for one major contingency: the failure of a poly-deposition system (causing a delay of about 8 days for repairs, and leading to an additional delay in wafer processing due to the Christmas holidays). At 10:00 am on Dec. 28, the type-B wafers completed fabrication. The ring oscillator test structures were probed and found to work. One project, Jim Clark's system-clock, was bonded and tested on the afternoon of Dec. 28, and was found to work completely. On Monday Dec. 31 the type-A wafers completed fabrication, and were found to be satisfactory. Packaging, bonding, document generation, and document printing proceeded through January 1. The shipments were mailed at 5:00 pm, January 2.

WHAT THE SHIPMENTS CONTAIN:

The shipment to each university contains (i) a collection of boxed, wire-bonded, packaged chips for that group of designers, (ii) a set of wire-bonding maps for those chips, marked-up to show the custom wire-bonding of each project, (iii) copies of the "MPC79 Implementation Documentation" to be distributed to all designers, and (iv) a questionnaire and return envelope for the designers, so that you all can provide us with some feedback. Coordinators should check to make sure that all this stuff is included in their school's shipment. This shipment provides each project coordinator with ONE packaged, wire-bonded chip for each PROJECT, and ONE set of documentation for each DESIGNER and for each STUDENT in the design course (including those who did not complete a design).

[Some unpackaged chips are also included in certain shipments. These can be packaged by the universities, and used by designers who need a second copy if they suspect that their first copy has manufacturing defects. We'll provide additional unpackaged chips later on. We can provide some additional packaged wire-bonded chips on request (depending on demand and timing); we'll expedite further packaging for those designers who are seriously testing their projects.]

DISTRIBUTING THE CHIPS AND DOCUMENTS:

Coordinators should carefully read Sections 2, 3, and 7 of the "MPC79 Implemention Documentation" before distributing the chips and the documentation to the designers.

Each boxed, packaged chip is marked with a code number. SECTION 2 of the Implementation Documentation describes how to associate these code numbers with the project ID's, so you can figure out which box belongs to which designers(s). SECTION 2 of the documentation also provides important warnings and tips about how to handle the chips and how to prepare them for testing. PLEASE request that designers READ SECTION 2 of the Implementation Documentation before doing anything with their boxed chips.

TESTING:

It is now up to you coordinators and designers to get those projects tested! Be sure to let us know how things went. We'd like to know which projects worked, and which ones didn't. Of the ones

that had bugs, we are very interested in the nature of the bugs, and also whether, and how, you figured out what went wrong. A short one-page questionnaire and a return envelope have been included for each student in the shipments. You can use these to send in your detailed test results. Try to get as many questionnaires back to us as possible before 31 January 1980. You can also send us test results by MSGs to MPC79@PARC-MAXC.

OUR PLANS FOR FURTHER DOCUMENTATION:

We are compiling a proceedings documenting the MPC79 effort, to be published as a Xerox PARC/SSL Report entitled: "Proceedings of the MPC79 Multi-University Multiproject Chip Set Project", edited by A.Bell, L.Conway, R.Lyon, M.Newell. This proceedings will include a general overview of MPC79, photos of various die types, information from the MPC79 ARPANET message traffic, information about the MPC Implementation System, and feedback from the universities.

We hope to include a collection of short-form project reports describing a number of the MPC79 projects (an example of such a report is included in the Implementation Documentation). Coordinators should especially encourage the designers of innovative projects to send us a report for the Proceedings (the deadline for reports is February 29, 1980). Designers may use the MPC79 questionnaires to let us know of their plans to submit a report.

The Proceedings will be printed in large quantities and distributed widely in the universities and in industry. We will send out copies to all participants. Instructors and coordinators: Make sure that your school is represented by some good reports in the Proceedings! For any of you designers who'd like some visibility, now's your chance!

PLANS FOR CHIP PHOTOS:

A commercial photographer will soon produce 8" x 10" photos, in color and in B/W, of each of the MPC79 die-types. We'll send some copies of these photos to each university, along with info on how to order more copies from the photographer, and how to arrange for individual project photos to be made.

LOOKING AHEAD:

Many of the MPC79 designers are already looking ahead, making plans for iterating their designs, and dreaming up more ambitious design projects. Many other university students will want access to VLSI implementation, so that they too can have the experience of learning to design in a state-of-the-art technology by actually doing it. The demand for such services may build rapidly, once folks know that it is feasible, and can visualize how small is the expenditure of resources per chip-set when compared to the value of the result to the community of designers. Thus, those designers who'd like to iterate their present designs, or take on a larger design, should take heart! There may be several MPC's in 1980! You instructors, coordinators, and designers can help to make sure this happens by letting other folks know what you've done, and how it was done. You can also help us

in this effort by submitting test results and short-form project reports for the MPC79 proceedings.

It is our sincere hope that MPC79 has provided a sufficient demonstration of the feasibility and practicality of remote-entry, fast-turnaround VLSI implementation, that it will lead to the funding and operation of a regular, scheduled VLSI implementation service for university students and researchers. We believe such a service will achieve an enormous return to the country on its investment, by greatly leveraging the human resources to be applied in the exploration of integrated system architecture and design.

ACKNOWLEDGEMENTS:

We wish to express our gratitude to all the folks who pulled together with us to make MPC79 happen, including our friends at Defense ARPA, at Micro Mask, and at Hewlett-Packard/ICPL.

We all owe a great deal to the dedication and efforts of the instructors and lab coordinators in the universities, who, working under great pressure and on a tight schedule, have done such a fantastic job with their design courses and project-labs this fall. We especially want to thank all the student designers for their enthusiastic response to the courses, and for their magnificent efforts and accomplishments on their VLSI system design projects. You have done well!

Organizing and carrying out the implementation of these many imaginative VLSI design projects has been a very exciting and rewarding experience for us here at Xerox PARC/SSL.

The MPC79 Organizers

Lynn Conway, Alan Bell, Martin Newell, Dick Lyon
LSI Systems Area, Xerox PARC/SSL
5 January 1980

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, CA 94304
February 28, 1980

To the MPC79 instructors
and project coordinators:

Dear Friends,

The photomicrographs of the MPC79 chip set have arrived! Enclosed with this shipment are several 8"x10" full-die photographs for you (in color, and in black and white) of each MPC79 die-type that contained projects from your university. Also enclosed are order forms that you and the participants can use to order either full-die photographs, or photographs of individual projects.

I'd appreciate it very much if you would post one set of these photos, and distribute the associated ordering information, so that the MPC79 participants at your university can obtain photos of their projects. Melgar Photographers, the firm that took the photos, specializes in IC photography. Their photographs are of high quality, a wide variety of sizes is available, and they are making the photos available to the MPC79 participants at a very nominal charge.

Also enclosed with this shipment are *Xerox color copies* of the MPC79 die-types containing projects from your university. Enough color copies are enclosed to provide each MPC79 participant from your university with a full set. These color copies don't have the resolution and quality of the original color photos, and certainly don't show as much detail of individual projects as will individual project photos ordered from Melgar. However, I think they will be of interest to the MPC79 participants, and I'd appreciate it if you would distribute them to as many MPC79 participants as possible at your university.

We are also sending (either with, or in parallel with, this shipment) some more unpackaged MPC79 chips for distribution to participants; there are about three chips in the shipment for each project from your school. If mounted in plastic boxes, these unpackaged chips provide a handy way to study the projects with microscopes, and make good souvenirs for the MPC79 participants.

We're working on the various MPC79 documents and reports, and will distribute copies of these to you as soon as they become available.

Sincerely,

Lynn Conway

Lynn Conway

MPC79 Photo Order:

MELGAR PHOTOGRAPHERS
2971 Corvin Drive, Santa Clara, CA 95051
February 28, 1980

To the MPC79 participants:

Melgar Photographers have recently taken photomicrographs of each of the die-types in the MPC79 Multiproject Chip Set. Prints of these photos can now be ordered by using the attached order form.

The photos can be ordered in color, or in black and white, in standard sizes ranging from 5"x7" up to 20"x24". Prices as a function of size and type are listed on the order form. We can also make prints as large as 40"x60"! (Contact us for price quotes on sizes larger than 20"x24").

The order form indicates two further options:

(i) Full Die Photographs: Full Die Photographs include the Starting Frame, and all projects within the Starting Frame, for a given Die-Type. These can be ordered by Die-Code (AB, AC, - - -, etc.).

(ii) Individual Project Enlargements: These are produced using the original Full-Die negatives. Such enlargements of individual projects can be ordered by Project-Code (AB-1, AB-2, - - -, etc.).

A map of the MPC79 Die-Types, and a list of the Project-Codes and corresponding Project ID's is given on the reverse side of this letter, for your convenience in determining the correct Die-Codes and Project-Codes for your order.

We will make the individual project enlargements at the quoted prices by using the original full-die negatives. This saves you from charges for rephotographing your individual project. In most cases, especially for the medium to large sized projects, this will yield good quality results. However, the smallest projects (for example AC-3) probably shouldn't be enlarged to more than about 8"x10".

We can produce the highest quality photomicrographs of individual projects, especially the smaller ones, by rephotographing the wafers to obtain full-sized negatives containing only single, individual projects. We have some MPC79 wafers on file, and can arrange to rephotograph individual projects on a custom basis; please contact us to discuss prices and make arrangements for such custom work.

If you have any questions about the procedures for ordering MPC79 photos, or about prices, please feel free to phone me at (408) 733-4500.

Yours truly,

Frank Saude

Frank Saude
President

ORDER FORM FOR MPC79 PHOTOGRAPHS:

To order photos of MPC79 Dies and/or individual Projects, complete this order form and mail to:

Melgar Photographers, 2971 Corvin Drive, Santa Clara, CA 95051.

Please make checks payable to *Melgar Photographers.* An example order is illustrated on the reverse side for your convenience. If you have any questions, contact Melgar at (408) 733-4500.

Unit Prices:

Size:	BW	Color
5"x7"	$2.25	$3.00
8"x10"	3.00	5.00
11"x14"	8.00	10.00
16"x20"	12.00	20.00
20"x24"	15.00	30.00

Customer Address:

Name:_____

Address:_____

City:_____

State:_____ZIP:_____

Phone:_____

Full Die Photographs: (Please print Die-Code carefully; an example code: AB)

QTY	Size	Color or BW	Die-Code	Unit Price	Total Price

Individual Project Enlargements: (print Project-Code carefully; example code: AB-8)

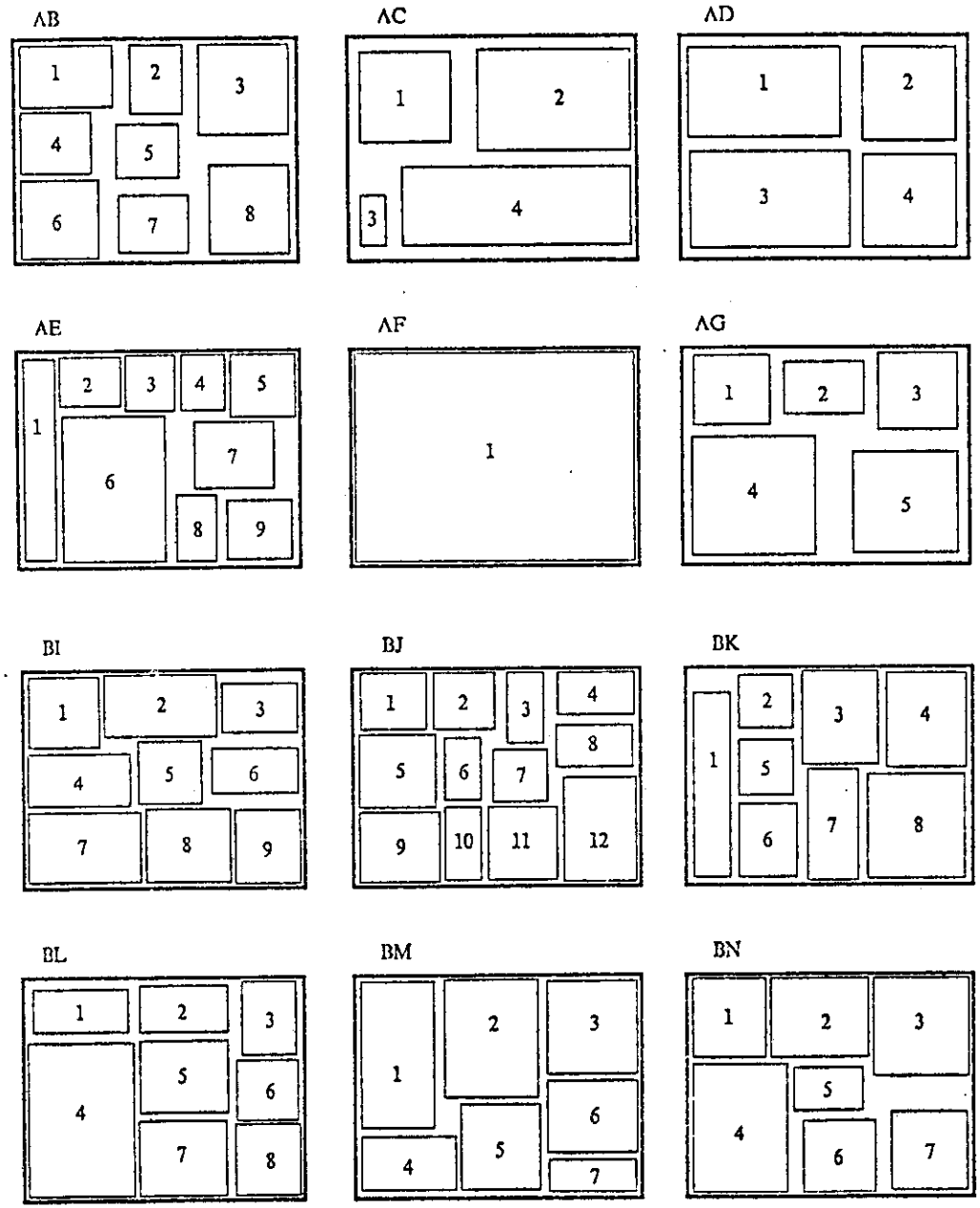
QTY	Size	Color or BW	Project-Code	Unit Price	Total Price

Subtotal: _____

+6.5% Sales Tax if CA order: _____

+2.50 for postage and handling: 2.50

Final Total: _____



MPC79 Multiproject Chip Layouts

(with Die-Codes)

List of Individual Project-Codes and corresponding Project ID's

Wafer MPC79A

AB-1 BataliMIT
AB-2 GramlichMIT
AB-3 FichtenbaumMIT
AB-4 KhouryMIT
AB-5 GoodrichMIT
AB-6 GrondalskiMIT
AB-7 PicardMIT
AB-8 AllenMIT

AC-1 HamiltonMIT
AC-2 PasemanMIT
AC-3 GlasserOT
AC-4 ChuMIT

AD-1 LuhukayUI
AD-2 HanesUI
AD-3 AdrianUI
AD-4 MontoyeUI

AE-1 GuptaCMU
AE-2 ClassUI
AE-3 MurrayOT
AE-4 RogersOT
AE-5 EbelingCMU
AE-6 KungCMU
AE-7 SongCMU
AE-8 HoeyCMU
AE-9 KehlOT

AF-1 Schip2

AG-1 WalpCT
AG-2 KathailMIT
AG-3 RivestMIT
AG-4 SnyderOT
AG-5 GoddeauMIT

Wafer MPC79B

BI-1 MacomberSU
BI-2 GehlbachSU
BI-3 MarkeeSU
BI-4 NoiceSU
BI-5 ElahianSU
BI-6 AtlasSU
BI-7 HerndonSU
BI-8 HannahSU
BI-9 WolffSU

BJ-1 CampbellCT
BJ-2 FuCT
BJ-3 PapachCT
BJ-4 LiCT
BJ-5 BartonCT
BJ-6 CocconiCT
BJ-7 PursifullCT
BJ-8 BozzutoCT
BJ-9 KingsleyCT
BJ-10 HoCT
BJ-11 WhitneyCT
BJ-12 TannerCT

BK-1 MathewsSU
BK-2 ZarghanSU
BK-3 FrolikSU
BK-4 BaskettSU
BK-5 Clark2SU
BK-6 OhChinSU
BK-7 BechtolsheimSU
BK-8 ClarkSU

BL-1 HellerCT
BL-2 EatonCT
BL-3 WatteyneCT
BL-4 MostellerCT
BL-5 GrayCT
BL-6 PinesCT
BL-7 DerbyCT
BL-8 PedersenCT

BM-1 LigockiCT
BM-2 DecuirUCB
BM-3 FungUCB
BM-4 LandmanUCB
BM-5 RumphCT
BM-6 EllisCT
BM-7 SequinUCB

BN-1 WatanabeUR
BN-2 LyonsUR
BN-3 KedemUR
BN-4 SohmUR
BN-5 TiloveUR
BN-6 UtiSU
BN-7 TarsiSU

AN EXAMPLE COMPLETED ORDER FORM:

ORDER FORM FOR MPC79 PHOTOGRAPHS:

To order photos of MPC79 Dies and/or individual Projects, complete this order form and mail to:

Melgar Photographers, 2971 Corvin Drive, Santa Clara, CA 95051.

Please make checks payable to *Melgar Photographers.* An example order is illustrated on the reverse side for your convenience. If you have any questions, contact Melgar at (408) 733-4500.

Unit Prices:

Size:	BW	Color
5"x7"	$2.25	$3.00
8"x10"	3.00	5.00
11"x14"	8.00	10.00
16"x20"	12.00	20.00
20"x24"	15.00	30.00

Customer Address:

Name: LYNN CONWAY

Address: 3333 COYOTE HILL RD.

City: PALO ALTO

State: CA ZIP: 94304

Phone: (415) 494-4316

Full Die Photographs: (Please print Die-Code carefully; an example code: AB)

QTY	Size	Color or BW	Die-Code	Unit Price	Total Price
1	8 x 10	BW	AF	3.00	3.00
2	8 x 10	Color	AF	5.00	10.00

Individual Project Enlargements: (print Project-Code carefully; example code: AB-8)

QTY	Size	Color or BW	Project-Code	Unit Price	Total Price
1	11 x 14	Color	BL-4	10.00	10.00

Subtotal: 23.00

+6.5% Sales Tax if CA order: 1.50

+2.50 for postage and handling: 2.50

Final Total: 27.00

MELGAR NEGATIVE NUMBERS:

(for Melgar internal reference use)

MPC79 DIE-CODE	BW NEGATIVE	COLOR NEGATIVE
AB	177112	177122
AC	1771-3	177124
AD	1771-7	177121
AE	177113	177127
AF	1771-5	177120
AG	1771-6	177119
BI	1771-9	177123
BJ	1771-8	177118
BK	177111	177129
BL	177110	177126
BM	177114	177125
BN	177115	177128

MPC79 Distribution Lists:

<Conway>MPC79.distribution:
November 11, 1979 11:31 AM

1. VIA the ARPANET:

Jacob Abraham, Univ. of Illinois, via DEWOLF@WPAFB-AFAL
Duane Adams, ARPA, Adams@USC-ISI,
Forest Baskett, FB@SU-AI,
Andy Bechtolsheim, AVB@SAIL,
Bob Brodersen, U. C. Berkeley, Brodersen@USC-ISI,
Randy Bryant, REB@MIT-XX,
Burt Bussell, UCLA, Bussell@UCLA-SECURITY,
Jim Cherry, Cherry@MIT-AI,
Jim Clark, CSL.JHC@SU-SCORE,
Danny Cohen, Cohen@ISIB,
Jerry Feldman, U. of R., Feldman@SUMEX,
Mike Foster, Foster@CMUA,
Ed Frank, Ed.Frank@CMUA
Lance Glasser, Lance@MIT-AI
Jack Holloway, H@MIT-AI,
Bob Hon, CMU, Hon@CMUA,
H.T. Kung, HT.Kung@CMUA,
Bob Kahn, ARPA, Kahn@USC-ISI,
Tom Knight, TK@MIT-AI,
Yngvar Lundh, NDRE, Yngvar@SRI-KA
Rob Mathews, ICL.ISL-ROB@SU-SCORE,
John Newkirk, ICL.ISL-NUKE@SU-SCORE,
Oddvar@SRI-KA
Bob Sproull, Sproull@CMUA,
Gerry Sussman, GJS@MIT-AI,
Joy Thompson, JOY@MIT-AI;

Notes: Jon Allen at MIT receives his MSGs via his secretary Joy Thompson; Most of the people on this ARPANET list are either involved in running the courses or in preparing research prototype designs, and thus need to be in touch in "real time" by MSGs.

2. VIA the Xerox National Alto Network:

Alan Bell, ABell.PA,
Bob Baldwin, Baldwin.PA,
Jim Baroody, Xerox WRC, Baroody.WBST,
Lynn Conway, Conway.PA,
Terri Doughty, Doughty.PA,
Doug Fairbairn, Fairbairn.PA,
Mark Kahrs, U. of R., Kahrs.PA,
Howard Landman, U.C.Berkeley, Landman.PA,
Dick Lyon, Lyon.PA,
Michael Nekora, Corp. R&D Staff, Nekora.PA,
Martin Newell, M-Newell.PA,
MPC79 files, MPC79.PA,
Don Oestreicher, Oestreicher.PA,
Rich Pasco, Pasco.PA,
Don Scharfetter, Scharfetter.PA,
Carlo Sequin, U.C.Berkeley, Sequin.PA,

Ted Strollo, Strollo.PA,
Bert Sutherland, Sutherland.PA,
Wayne Wilner, Wilner.PA;

Notes: Most of the people on this list are either LSI Systems Area staff or are Xerox observers of MPC79; however, we do reach some university folks via the Alto Network.

3. VIA the US MAIL:

There are a number of people in the participating organizations and in the universities who are being copied on selected MSGs by mail so that they can visualize what is happening and can follow the progress of this effort:

Jacob Abraham, Univ. of Illinois, (back-up copy)
Merrill Brooksby, HP
Irene Buchanan, Univ. of Edinburgh
Pat Castro, HP
Vir Dhaka, Xerox MEC
Russ Hill, Micro Mask
Dave Hodges, U. C. Berkeley
Ted Kehl, Univ. of Washington
Dan Lewis, Univ. of Santa Clara
Rob Mathews, Stanford (back-up copy)
Carver Mead, Caltech
Jim Meindl, Stanford
John Murray, Univ. of Colorado
John Newkirk, Stanford (back-up copy)
Richard Newton, U. C. Berkeley
Paul Penfield, MIT
Fred Rosenberger, Washington Univ.
Chuck Seitz, Caltech
Carlo Sequin, U.C.Berkeley, (back-up copy)
Kent Smith, Univ. of Utah
Ivan Sutherland, Caltech
Craig Wegl, Micro Mask

MPC79.distribution: ABell.PA, Adams@USC-ISI, AVB@SAIL, Baldwin.PA, Baroody.WBST, Brodersen@USC-ISI, Bussell@UCLA-SECURITY, Cherry@MIT-AI, Cohen@ISIB, Conway.PA, CSL.JHC@SU-SCORE, DEWOLF@WPAFB-AFAL, Doughty.PA, Ed.Frank@CMUA, Fairbairn.PA, FB@SU-AI, Feldman@SUMEX-AIM, Foster@CMUA, GJS@MIT-AI, H@MIT-AI, Hon@CMUA, HT.Kung@CMUA, ICL.ISL-NUKE@SU-SCORE, ICL.ISL-ROB@SU-SCORE, Irene.Buchanan@CMU-10D, JOY@MIT-AI, Kahn@USC-ISI, Kahrs.PA, Lance@MIT-AI, Landman.PA, Lyon.PA, M-Newell.PA, MPC79.PA, Nekora.PA, Oddvar@SRI-KA, Oestreicher.PA, Pasco.PA, REB@MIT-XX, Scharfetter.PA, Sequin.PA, Sproull@CMUA, Strollo.PA, Sutherland.PA, TK@MIT-AI, Wilner.PA, Yngvar@SRI-KA;

Jacob Abraham
College of Engineering
Coordinated Science Laboratory
University of Illinois
Urbana, Illinois 61801

Prof. Jonathan Allen
Massachusetts Institute of Technology
EE/CS Department, Rm 36-575
77 Massachusetts Ave.
Cambridge, MA 02139

Merrill Brooksby
Hewlett-Packard
Bldg. 28
1501 Page Mill Road
Palo Alto, CA 94304

Irene Buchanan
Department of Computer Science
University of Edinburgh
JCMB, Kings Bldgs., Mayfield Road
Edinburgh EH9 3JZ, Scotland, U.K.

Patricia L. Castro
Operations Manager, IC Laboratory
Hewlett-Packard Laboratories
3500 Deer Creek Road
Palo Alto, CA 94304

Vir Dhaka
Xerox Corporation
701 So. Aviation Blvd. M217/244A
El Segundo, CA 90245

Prof.Dr.Ing. Reiner W. Hartenstein
FB Informatik
University of Kaiserlautern
D-6750 Kaiserlautern
Federal Republic of Germany

C. Russ Hill
Micro Mask, Inc.
695 Vaqueros Ave.
Sunnyvale, CA 94086

Bob Hon
Carnegie-Mellon University
Department of Computer Science
Schenley Park
Pittsburgh, Pennsylvania 15213

Dr. Robert E. Kahn
Advanced Research Projects Agency
1400 Wilson Boulevard
Arlington, VA 22209

Mark Kahrs
University of Rochester
Computer Science Department
Rochester, N.Y. 14627

Prof. Ted Kehl
Dept. of Computer Science, FR-35
University of Washington
Seattle, WA 98195

Prof. H.T. Kung
Carnegie-Mellon University
Department of Computer Science
Schenley Park
Pittsburgh, Pennsylvania 15213

Prof. Dan Lewis
Dept. EECS
University of Santa Clara
Santa Clara, CA 95053

Prof. Rob Mathews
AEL 201
Stanford Elec. Labs
Stanford University
Stanford, CA 94305

Prof. James Meindl
AEL 118
Stanford Elec. Labs
Stanford University
Stanford, CA 94305

Prof. John Murray
EE/CS Department
University of Colorado
Colorado Springs, Colorado 80907

Prof. John Newkirk
AEL 201
Stanford Elec. Labs
Stanford University
Stanford, CA 94305

Prof. Paul Penfield, Jr.
Massachusetts Institute of Technology
EE/CS Department, Rm 36-377
77 Massachusetts Ave.
Cambridge, MA 02139

Prof. Ron Rohrer
Chairman
Electrical Engineering Department
Southern Methodist University
Dallas, Texas 75275

Prof. F. U. Rosenberger
Computer Systems Laboratory
724 South Euclid Avenue
Washington University
St. Louis, MO 63110

Dr. Charles L. Seitz
Computer Science, 256-80
California Institute of Technology
Pasadena, CA 91125

Prof. Carlo Sequin
EE/CS Department
CS Div., 529A Evans Hall
University of California
Berkeley, CA 94720

Prof. Kent Smith
Computer Science Dept.
3160 Merrill Engineering Bldg.
University of Utah
Salt Lake City, Utah 84111

Prof. Robert Sproull
Carnegie-Mellon University
Department of Computer Science
Schenley Park
Pittsburgh, Pennsylvania 15213

Prof. Ivan Sutherland
Computer Science, 256-80
California Institute of Technology
Pasadena, CA 91125

Craig A. Wegl
Micro Mask, Inc.
695 Vaqueros Ave.
Sunnyvale, CA 94086

MPC79 University Info, 9-30-79:

The Fall '79 Multiuniversity Multiproject Chip Set: Planning Information:
Filed on <Conway>MPChip.info
September 30, 1979 3:53 PM

Information Management and Implementation Management: LSI Systems Area, Xerox PARC.
Maskmaking: Micro Mask, Inc.
Wafer Fabrication:
Participating Universities: M.I.T., Stanford, Caltech, CMU, University of Rochester

M.I.T.
Dept. of Electrical Engineering and Computer Science
77 Massachusetts Avenue
Cambridge, Massachusetts 02139
617/253-1000 (Main MIT #)

File Transfer Account:	[MAXC]<MIT-VLSI>	Account managed by: Randy Bryant
VLSI Design Course:	6.371	Meets: Tue/Thu 2:00-3:30
Instructor(s):	Jon Allen 617/253-2509	
Teaching Assistant(s):	Randy Bryant	
Students:	30: mostly grad students, a few undergrads, 2 from BBN, 2 from GenRad	

Send MPChip informational MSGs to:

Randy Bryant		REB@MIT-XX
Tom Knight		TK@MIT-AI
Jack Holloway		H@MIT-AI
Joy Thompson (sec'ty)	617/253-7309	JOY@MIT-AI

Other contacts:

Lance Glasser	617/253-7309	
Jerry Roylance		GLR@MIT-AI
Jim Cherry		Cherry@MIT-AI

Stanford University

File Transfer Account:	[MAXC]<SU-VLSI>	Account managed by:	John Newkirk
VLSI Design Course:	EE292V	Meets: Tue/Thu 9:45	
Instructor(s):	Rob Mathews, John Newkirk		
Teaching Assistant(s):			
Students:	~100		

Send MPChip informational MSGs to:

John Newkirk	415/497-0548	NUK@SU-AI
Rob Mathews		BOB@SU-AI
Forest Baskett	415/497-1916	FB@SU-AI

Other contacts:

Jim Clark	415/497-1414	CSL.JHC@SU-SCORE

Caltech

Computer Science, 256-80
Pasadena, California 91125
213/795-6811, X2841

File Transfer Account:	[MAXC]<Caltech-VLSI>	Account managed by:	Doug Fairbairn
VLSI Design Course:	CS/EE181a	Meets Tue/Thu 1:30-3:00	
Instructor(s):	Doug Fairbairn, Rm 272		
Teaching Assistant(s):	Dick Lang, Greg Eflan		
Students:	43: ~1/2 seniors, 1/2 1st yr grads, 3 from Xerox, several from the SSP.		

Send MPChip informational MSGs to:

Doug Fairbairn	213/795-6811, X2549	Fairbairn@PARC-MAXC

CMU

Department of Computer Science
Schenley Park
Pittsburgh, Pennsylvania 15213
412/578-2000

File Transfer Account: [MAXC]<CMU-VLSI> Account managed by: Bob Hon
VLSI Design Course: - - -
Instructor(s): - - -

Note: The CMU course is offered in the Spring Semester. However, a number of CMU research project LSI designs will be merged into this MPChip.

Send MPChip informational MSGs to:

Bob Hon	412/578-3056	Hon@CMUA
Bob Sproull	412/578-2621	Sproull@CMUA

Other contacts:

HT. Kung	412/578-2568	HT.Kung@CMUA

University of Rochester
Computer Science Department
Rochester, New York 14627
716/275-5671 (C.S.Dept.)

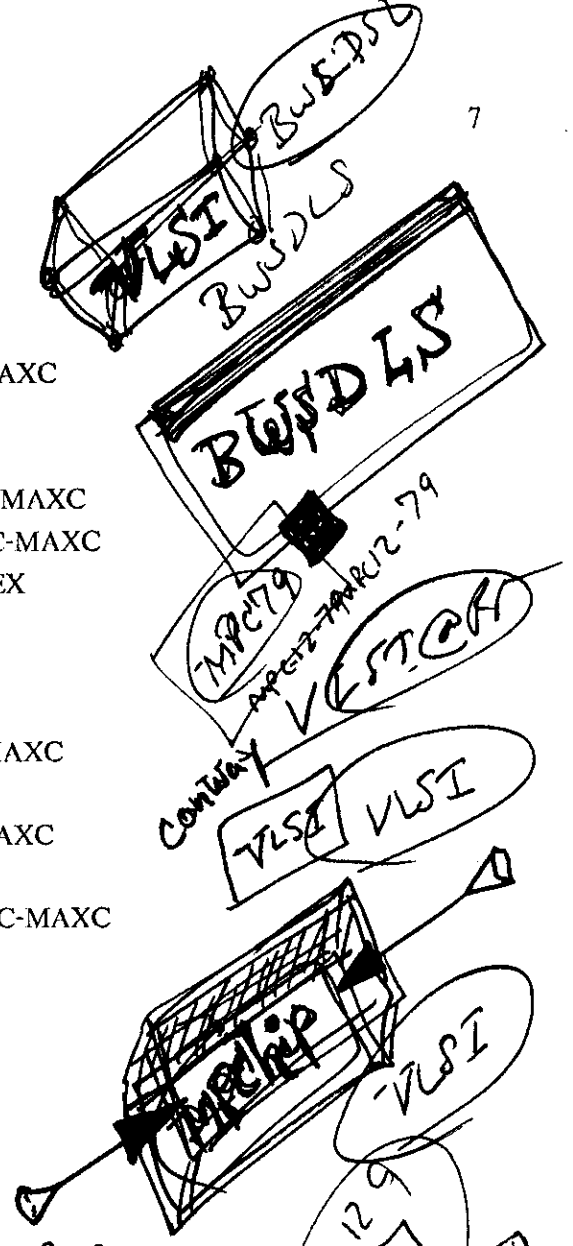
File Transfer Account:	[MAXC]<UofR-VLSI>	Account managed by:	Mark Kahrs
VLSI Design Course:	?	Meets: ?	
Instructor(s):	?		
Teaching Assistant(s):	Mark Kahrs		
Students:	?		

Send MPChip informational MSGs to:

Mark Kahrs	716/275-5766 (w)	Kahrs@PARC-MAXC	716/442-6404 (h)
Jerry Feldman		Feldman@SUMEX	
Jim Baroody	8-222-6437	Baroody	

MPChip ARPANET Informational MSG List:

Jim Baroody		Baroody
Forest Baskett	415/497-1916	FB@SU-AI
Alan Bell	415/494-4326	ABell@PARC-MAXC
Randy Bryant		REB@MIT-XX
Jim Cherry		Cherry@MIT-AI
Lynn Conway	415/494-4316	Conway@PARC-MAXC
Doug Fairbairn	213/795-6811, X2549	Fairbairn@PARC-MAXC
Jerry Feldman		Feldman@SUMEX
Jack Holloway		H@MIT-AI
Bob Hon	412/578-3056	Hon@CMUA
Bob Kahn		Kahn@USC-ISI
Mark Kahrs		Kahrs@PARC-MAXC
Tom Knight		TK@MIT-AI
Dick Lyon	415/494-4325	Lyon@PARC-MAXC
Rob Mathews		BOB@SU-AI
Martin Newell	415/494-4328	M-Newell@PARC-MAXC
John Newkirk	415/497-0548	NUK@SU-AI
Bob Sproull	412/578-2621	Sproull@CMUA
Joy Thompson	617/253-7309	JOY@MIT-AI



Carlo Seguin 415/642-5103 Seq..n@PARC-MAXC
Gerry Sussman GJS@MIT-AI
Landman.PA

Yngvar@SRI-KA
Oddvar@SRI-KA

Vir Dhaka MEC <ESmail>

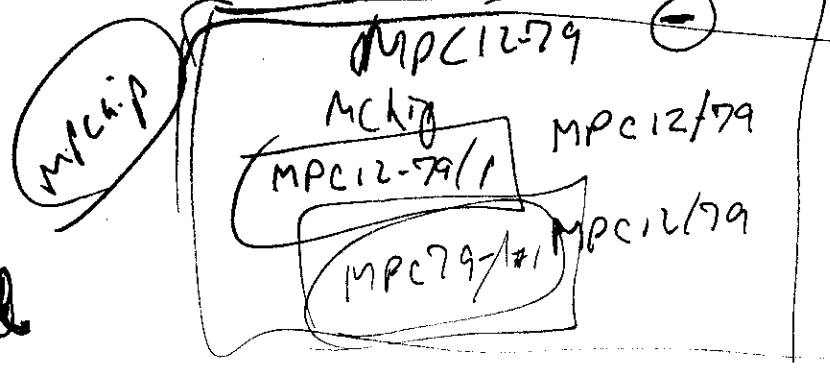
Vir Dhaka

Irene Buchanan

Pake

Spinrad

Sutherland



MPChip Hardcopy Informational MSG List:

Murray (Colorado)

Jacob Abraham (Illinois)

Irene

Ted Kehl ?

The ARPA community

Vir Dhaka

B

Carlo

MPC79 University Info, 10-31-79:

INFORMATION FILE ON THE UNIVERSITY COURSES:

Filed on <Conway>university.info October 31, 1979 6:35 PM

1. Courses now underway or to be offered later-on this school year:

M.I.T.

Dept. of Electrical Engineering and Computer Science
77 Massachusetts Avenue
Cambridge, Massachusetts 02139

Course Number/Name:	6.371, "Introduction to VLSI Systems"
Instructor(s):	Jonathan Allen , 617/253-2509; Paul Penfield (also lecturing?).
Teaching Assistant(s):	Randy Bryant, REB@MIT-XX
Meets:	Fall Semester, Tue/Thu 2:00-3:30
Students:	30: mostly grad students, a few undergrads, 2 from BBN, 2 from GenRad

Stanford University

Course Number/Name:	EE292V, "Introduction to VLSI Systems"
Instructor(s):	Rob Mathews, Bob@SU-AI; John Newkirk, NUK@SU-AI, 415/497-0548
Teaching Assistant(s):	
Meets:	Fall Semester, Tue/Thu 9:45
Students:	71 registered, ~40 auditors

Caltech

Computer Science, 256-80
Pasadena, California 91125
213/795-6811, X2841

Course Number/Name:	CS/EE181a
Instructor(s):	Doug Fairbairn, Fairbairn@PARC-MAXC, 213/795-6811, X2549
Teaching Assistant(s):	Dick Lang, Greg Eflan
Meets	Fall Semester, Tue/Thu 1:30-3:00
Students:	43: ~1/2 seniors, 1/2 1st yr grads, 3 from Xerox, several from the SSP.

CMU

Department of Computer Science
Schenley Park
Pittsburgh, Pennsylvania 15213
412/578-2000

Course Number/Name:		
Instructor(s):	Bob Sproull, Sproull@CMUA, 412/578-2621	
Teaching Assistant(s):		
Meets	Spring Semester	
Students:	~20	
Other contacts:		
HT. Kung	412/578-2568	HT.Kung@CMUA
Bob Hon	412/578-3056	Hon@CMUB

University of Rochester

Computer Science Department
Rochester, New York 14627
716/275-5671 (C.S.Dept.)

Course Number/Name:	EE492/CS492
Instructor(s):	Group of EE and CS faculty
Teaching Assistant(s):	Mark Kahrs, 716/275-5766 (w), Kahrs@PARC-MAXC
Meets:	Fall Semester
Students:	14 + some auditors; several students are from Xerox WRC

University of California, Berkeley

EECS Department, Computer Science Division
Berkeley, California 94720

Course Number/Name:	CS248, "MOS LSI Design"
Instructor(s):	Carlo Sequin, Sequin@PARC-MAXC, 415/642-5103
Teaching Assistant(s):	
Meets:	Winter quarter
Students:	~40 to 50

University of Utah

Computer Science Department
3160 Merrill Engineering Bldg.
Salt Lake City, Utah 84111
801/581-

Course Number/Name:
Instructor(s): Kent Smith,
Teaching Assistant(s):
Meets: Fall-Winter-Spring 3-quarter sequence
Students:

University of Colorado,

EE/CS Department,
College of Engineering and Applied Science
Colorado Springs, Colorado 80907
303/598-3737

Course Number/Name:
Instructor(s): John Murray, X285 (now organizing course)
Teaching Assistant(s):
Meets: Spring semester (probably)
Students: ~20

University of Illinois

Department of Electrical Engineering
Urbana, Illinois 61801

Course Number/Name:
Instructor(s): Jacob Abraham, 217/333-0750
Teaching Assistant(s):
Meets: Fall Semester (ends ~21 Dec)
Students: 15
Notes: This is the first, experimental offering of the course at Univ. of Illinois. The course will be run again in the spring of '80, for about 40 students.

University of Washington

Computer Science Department, Sieg Hall
Seattle, Washington 98195
206/543-1695

Course Number/Name: CS590
Instructor(s): Ted Kehl, 206/543-2424
Teaching Assistant(s):
Meets: Fall semester
Students: 15, grad students and faculty members
Notes: Using LAP on a DECsystem20 + HP7221A

Universitat Kaiserslautern

FB Informatik
D-6750 Kaiserslautern
Fed. Rep. Germany
01149-631-854-2606

Course Number/Name: "Einfuhrung in VLSI Entwurf"
Instructor(s): Reiner Hartenstein, Peter Liell, Michael Flototto
Teaching Assistant(s):
Meets: Winter-semester, Freitag 10.00-12.00
Students: 20 experienced students

This fall Prof. Hartenstein will also begin a 3 semester electronic-design course-sequence for undergraduates, which will introduce basic logic-design this fall, electronic-circuits, semiconductor fundamentals, and basic nMOS circuits in the spring, leading finally to a large number of undergraduate students taking the VLSI design course next fall.

University of Edinburgh

Department of Computer Science
James Clerk Maxwell Bldg., Kings Buildings, Mayfield Road
Edinburgh EH9 3JZ, Scotland, U.K.

Course Number/Name:
Instructor(s): Irene Buchanan, Buchanan@CMUD (temporarily)
Teaching Assistant(s):
Meets: Winter Quarter(~Jan-Mar)
Students:
Notes: Martin Newell talked to Irene by phone 10-17; she confirmed her plan to teach the course. She will be in MSG contact via the ARPANET very soon. She plans to prepare a design for MPC79. Sounds like she has caught the fever!

2. Courses will probably/possibly be offered during this school year at :

S.M.U.

Electrical Engineering Department
School of Engineering and Applied Science
Dallas, Texas 75275
214/692-3106

Course Number/Name:
Instructor(s): Ken Heizer
Teaching Assistant(s):
Meets: Spring Semester
Students:
Note: This course will also be shown over the TAGER TV network.

Washington University

Computer Systems Laboratory
724 South Euclid Ave.
St. Louis, MO 63110

Course Number/Name:
Instructor(s): Fred Rosenberger?, 314/454-3395, 361-7356
Teaching Assistant(s):
Meets:
Students:

U.S.C.

Course Number/Name:
Instructor(s): John Nelson? (took the Wash. Univ. teacher's course)
Teaching Assistant(s):
Meets: Have report that course will be offered in the spring of '80
Students:

Union College (rumor, not yet checked out)
EE/CS Department
Schenectady, NY

Course Number/Name:
Instructor(s): George Williams? (took the Wash. Univ. teacher's course)
Teaching Assistant(s):
Meets:
Students:

U.C.L.A.
Prof. Burt Bussell
Computer Science Dept.
Boelter Hall 3731
U.C.L.A.
Los Angeles, California 90024

Course Number/Name: CS259/ES&E219A
Instructor(s): Vance Tyree, JPL; Boelter Hall 3731g, UCLA
Teaching Assistant(s):
Meets:
Students: 9 Registered, 6 Auditors
Contact: Prof. Burt Bussell, Vice-Chairman, CS Dept.
Bussell@UCLA-SECURITY

MPC79 Notes:

THINGS TO COME IN MPC79

- ⊙ MESSAGE #3: REQ ↔ ACK game — Lynn, Alan
- LIBRARY DOCUMENTATION (overglassing?) — Dick
- MESSAGE #4: Copyrights, ---, Logos, ---
  "How to think of your design" and the publishing analogy — Lynn
- MESSAGE #6: Space War: The Rules, Guidelines.
- MESSAGE #7: Details: Packaging, no overglassing, --
  Note: Be able to get BB easily
- CIF: MESSAGE #4: warnings & tradeoffs on use of wires, polygons, etc. DD's? Symb. #5. — within Dick

→ Meet with HP on 30 Oct

- λ, thresholds, oxide thickness, nMOS silicon gate Dyad
- NO OVERGLASSING
- NO SUBSTRATE BIAS (needed)
- VDD = 5 ✓
- Shuttle Frame: Align Marks, Test Patterns
- → MASK POLARITY (Get info before meeting)
- Relative Time Schedule to keep going at full speed.
- Quantity: 2 masks set, etc.
- MASK PLATE TYPE: Thickness, mtls

HP meeting Preparation:

SHOW THEM OUR STARTING FRAME STUFF

- ALIGNMENT MARKS (esp if POS resist used)
- LAYER NAMES
- SCRIBE LINES
- EXAMPLE LOGOS
- DISCRETE TRANS. TEST PATTERNS
- ETCH TESTERS
- C/D's

HAVE DATA

4x4x[illegible]mils AR-CHROME

- Mask Types: Thickness, materials, etc.

Questions:
- Resist Polarities (mask polarities) (All Negative Resist)
- Scribes lines OK?
- Really Confirm $\lambda = 2.5\mu m$ ✓
- Stretches & Shrinks?
- Confirm 2 mask sets & start 4B/set.

FACTS ABOUT MPC79

- NO OVERGLASSING (?) Test Lot, Lot w/o

[redacted]

- No Buried contacts.

HOW TO HANDLE CONTINGENCIES (TIME)

EX: MICRO MASK SLOW OR SOFTWARE DIFFICULTIES:

SOLN: STAGGER MASK SETS OR MASKS WITHIN A SET.

- QUESTION: In what order do they need MASKS?
- " " : What are relative dates?
- We're going to try for poor bit TA – but no test on them: best guess should be easy to beat.

PROCESS: Get Them Standard nMOS Basic Specs OK.

- VDD = 5V ✓
- nMOS, depl. mode loads, silicon gate ✓
- [redacted] substrate bias: like to be able to run OK without.
- V_{th} ~ 0.2 VDD ; V_{thp} ~ −0.6 ÷ 8 VDD
- Oxides: NSILI 1100 Å NSILII 700 Å
- Poly : " " 3200 Å
- Metal : ?
- How they prepare the back side of wafers, what state in for use of conducting epoxy?
- Mean, Var of Poly Ω/□ ? estimate?

GET SAMPLE MASK INTERFACE FORMS TO SHOW THEM. CHECK IF NEED ANY FACTS FROM THEM. [ALAN: get the "water MAPS"]

HAVE DATA

GIVE TO HP FOLKS

- MIT Blurb
- PARC Blurb
- (SHOW IMPL. GUIDE) - maybe leave outside
- Hardcopies of MSGs.
- ARPANET DIRECTORY

GIVE THEM

PARTICIPANTS: ALL Registered in Univ. Courses, except for (i) some faculty members (ii) Xerox-MIT Scheme Chip. (iii MIT ow's)

We'll probably build a Logo + "participants' conf." files to include in starting Frame.

Meet Merrill Brooksby at Artjive, Thursday 4 Oct at 11:30.

CONTACT MERRILL BROOKSBY

H.P. 1501 Page Mill Rd. Palo Alto CA 94304

Main Number: 415/~~493-1501~~ 856-1501
Merrill's # 856-4170

- Talked to Jon Allen. He indicated HP might be int. in a collaboration similar to last year.
- I thought I'd outline our plans - give you a feeling for the overall effort. Then perhaps you could discuss this with HP Dear Creek to see if it might be possible. (MIT, STANFORD, CALTECH, CMU, UNIV. OF ROCH.) ~ 100 projects.
- One important thing: We are quite flexible in our notion of how to provide the front-end software ... we'd be pleased to have some of your technical people interact with us --- sit in on the technical sessions here, if that could be of interest.
- General idea: from HP Dear Creek's point of view, the effort could appear very similar to last year's. Probably one week set. ~ same # writers run.
- We have greatly improved all the rest of the procedure, so HP will not be under great pressure to do all that a thousand as last year. Even if it took twice as long, the overall time will be less.
- If you confirm an interest - I suggest we plan on a meeting here at PARC for us to describe in general plan and have our technical people get to know each other, so they can work out the further details of defining the machine interface for this years run.

	School	Die	# Projects	Shipment: color plates	BW plates	order forms	color copies		Send to
✓ sent	MIT	B	8	3	3	50	40		RANDY
		C	3	3	3		40		
		G	3	3	3		40		
		F	1	3	3		40		
✓ sent to Doug	CALTECH	J	12	3	3	50	40		DOUG
		L	8	3	3		40		
		M	3	3	3		40		
		G	1	3	3		40		
✓ sent	STANFORD	I	9	3	3	60	60		ROB
		K	8	3	3		60	+	20
		N	2	3	3		60		
✓ sent	CMU	E	5	3	3	10	20		KUNG
✓ sent	UCB:	M	4	2	2	5	10		CARLO
✓ sent	Illinois	D	4	2	2	5	20		JACOB
		E	1	2	2		20		
✓ sent	ROCHESTER	N	5	3	3	15	20		Feldman
✓	Kehl	E	1	1	1	2	3		
	Murray	E	1	1	1	2	3		
	Rogers	E	1	1	1	1	3		
✓	Snyder	G	1	2	2	2	4		

MPC79 Area Estimates:

ESTIMATES: 11-28-79

	Caltech	~120 mm²	23 projects	25 des.
	CMU	~30 mm²	5 proj.	6 des.
	Univ. of Ill.	~36 mm²	7	12 des.
→	SU	~50 to 100 mm²	6-15	8-20 des
	UCB	~16 mm²	3	5
(Schlaer?)	U of R	~15 mm²	4	8
	MIT	~120 mm²	20	30
(Snyder?)	U of W	~15 mm²	3	7
	Scheme	~45 mm²	1	4

(E+Δ) probable max	~472 mm²	~77 projects	~111 designers
(E) expected value	~450	~70	~100
(E-2Δ) possible min	~400	~60	~80

DIE TYPES (LESS DOC.): MIN ~10; MAX ~12

Area	School	#proj. ACH	Area (# dec)		Other info
(6.89)	MIT	19	130.99	32	(2 more might come: 4.0 + 3.5 = 7.5)
(5.66)	CMU	5	28.32		——— (4)
	OTHER	2	56.19		(3 more likely ✓ 3 + 3 + 3 = 9)
(5.22)	CALTECH	26	135.71	33	(likely to lose 3 or 4 ✓ = −10)
(6.97)	ILLINOIS	6 (5)	41.83		(2 more poss. blr 4 + 3 = 7)
	U of R	0	0		(?) 60 B max est. ~10
(4.5)	UCB	2	8.99		likely one more = 9.
(4.95)	STANFORD	19	94.17	36	36.7 pending (=6 will make it)
		79	496.15		21

2 DEC ESTIMATES

MIT

5.51
4.27
0.87 (?)
13.13
14.11
6.25
8.65
2.88
2.83
4.84
6.25
1.06
3.45
4.00
13.07
3.38
29.49
1.89
5.06

130.99

(other)

est 4.0 not ready yet
est 3.5 " " "

19

5

CMU

3.44
5.70
2.35
12.48
4.35

28.32

Other

44.73
11.46

56.19

(Other)

Boyd ?
Glosser ?
Kehl 3.2
Rogers !
+ (N 3)

(2)

U of I

13.38

2.57

6.94

1.07

11.30

6.57

41.83

No design

3.00

4.00

7.00

SU

3.41

6.09

4.81

2.92 (Clark254)

8.23

3.44

5.90

5.23

5.11

7.31

3.02

5.87

4.55

3.60

5.90

7.64

4.63

4.00

19 2.46
94.12

2.81 Ahmed —

4.39 Erbil —

5.84 Frolik ✓ (*)

4.25 Honomite

4.00 Huang

4.25 Kaiser...

3.61 McCorkle

7.50 Oyc

36.65

x	y
309	309
309	309
314	314
310	311
311	312
308	309
312	314
313	314
313	314
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312	313
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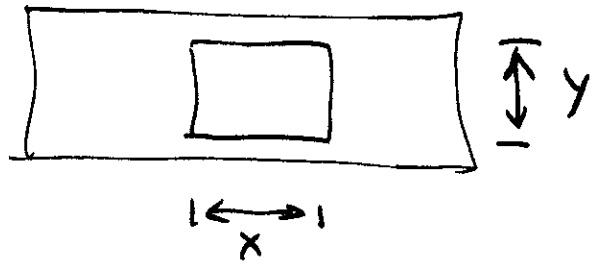
313	313
308	312
312	315
314	313
314	312
310	310
313	313



CORRECT BY -1 to -2

say BY (-2) to be safe:

Summary: overall and max:

310

	-4	-3	-2	-1	0	1	2	3
overall	2	5	3	3	10	7	9	1
max		3	1		4	3	8	1

MPC79 University Merges:

Memo from: LYNN CONWAY

UCB SUMMARY

4 proj.	21.81 mm^2

XEROX

Summary of designs from UCB, updated 4-Dec-79 20:40:30

✔DecuirUCB

Designers: J. Decuir, C.H.Sequin
Description: squareroot of 3 approximator for
radix-3 block in FFT computer
BOUNDS: 265000 327750 132500,163875

Design is awaiting allocation.
Required space = 2650 x 3278 microns, Area = 8.69 sq mm
Priority time: 4-Dec-79 13:13:22
Current submittal is acceptable for implementation.
File name: [Maxc]<SEQUIN>DECUIRUCB.;2
File creation date: 4-Dec-79 13:13:22
Bounding box = 2650 x 3278 microns, Area = 8.69 sq mm

✔FungUCB

Designers: W.-C. Fung, C.H.Sequin
Description: general purpose barrel shifter for sraggered ,
pipelined data in an FFT computer
BOUNDS: B 248250 265000 124125,132500

Design is awaiting allocation.
Required space = 2484 x 2650 microns, Area = 6.58 sq mm
Priority time: 3-Dec-79 20:30:14
Current submittal is acceptable for implementation.
File name: [Maxc]<SEQUIN>FUNGUCB.;2
File creation date: 3-Dec-79 20:30:14
Bounding box = 2484 x 2650 microns, Area = 6.58 sq mm

✔LandmanUCB

Designer: Howard A. Landman
Description: This project is a reprogrammable PLA, with
8 each inputs, pterms, and (tri-state) outputs.
Est.BB: ~2600 x 1600 microns

Design is awaiting allocation.
Required space = 2600 x 1590 microns, Area = 4.13 sq mm
Priority time: 3-Dec-79 12:20:29
Current submittal is acceptable for implementation.
File name: [Maxc]<LANDMAN>MPC79-LANDMANUCB.CIF;1
File creation date: 3-Dec-79 12:20:29
Bounding box = 2600 x 1590 microns, Area = 4.13 sq mm

✔SequinUCB

Designer Carlo H. Sequin
Description: Dual 16-stage FIFO with double rail signalling
Est BB: 2460 980

Space is allocated.
Reserved space = 2460 x 980 microns, Area = 2.41 sq mm
Priority time: 5-Nov-79 10:47:48
Current submittal is acceptable for implementation.
File name: [Maxc]<SEQUIN>SEQUINUCB.CIF;1
File creation date: 5-Nov-79 10:47:48
Bounding box = 2460 x 980 microns, Area = 2.41 sq mm

Memo from: LYNN CONWAY

What happened to Me.Doc ?

~CALTECH SUMMARY

~~22~~ 23 proj.	94.28 mm^2

+ HIT LIST :

1 proj.	9.83 mm^2

XEROX

CALTECH FINAL

Summary of designs from CalTech, updated 4-Dec-79 22:28:11

✔ BartonCT

Designer(s): Eric Barton
Description: LED array driver
Est.BB: ~2125 x 2125 microns

Space is allocated.
Reserved space = 2126 x 2126 microns, Area = 4.52 sq mm
Priority time: 26-Nov-79 22:33:35
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BARTONCT.CIF;2
File creation date: 3-Dec-79 23:33:26
Bounding box = 2126 x 2126 microns, Area = 4.52 sq mm

✔ BozzutoCT

Designer(s): Rick Bozzuto
Description: Pulse width to binary converter
Est.BB: ~1500 x 2300 microns

Space is allocated.
Reserved space = 2120 x 1288 microns, Area = 2.73 sq mm
Priority time: 26-Nov-79 22:35:51
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BOZZUTOCT.CIF;1
File creation date: 3-Dec-79 23:51:28
Bounding box = 2120 x 1288 microns, Area = 2.73 sq mm

✔ CampbellCT

Designer(s): James Campbel
Description: Logical processing unit with internal registers
Est.BB: ~1400 X 1400 microns

Space is allocated.
Reserved space = 1856 x 1704 microns, Area = 3.16 sq mm
Priority time: 27-Nov-79 0:03:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>CAMPBELLCT.CIF;2
File creation date: 3-Dec-79 23:38:10
Bounding box = 1856 x 1704 microns, Area = 3.16 sq mm

✔ CocconiCT

Designer: Alan Cocconi
Description: array processor
Est.BB: 2000 x 2000 microns

Space is allocated.
Reserved space = 1896 x 1074 microns, Area = 2.04 sq mm
Priority time: 1-Dec-79 20:20:33
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>COCCONICT.CIF;3
File creation date: 4-Dec-79 15:02:38
Bounding box = 1896 x 1074 microns, Area = 2.04 sq mm

✔ DerbyCT

Designer(s): Howard Derby
Description: Associative Memory
Est.BB: ~2250 x 2250 microns

Design is awaiting allocation.
Required space = 2170 x 2566 microns, Area = 5.57 sq mm
Priority time: 26-Nov-79 22:39:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>DERBYCT.CIF;4
File creation date: 4-Dec-79 15:04:56
Bounding box = 2170 x 2566 microns, Area = 5.57 sq mm

✔ EatonCT

Designer(s): Steve Eaton
Description: Counter/adder
Est.BB: ~ 1400 x 2600 microns

Space is allocated.
Reserved space = 2500 x 1376 microns, Area = 3.44 sq mm
Priority time: 26-Nov-79 23:14:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>EATONCT.CIF;2
File creation date: 3-Dec-79 23:53:13
Bounding box = 2500 x 1376 microns, Area = 3.44 sq mm

✔ EllisCT

Designer(s): Mike Ellis
Description: Stepping motor controller
Est.BB: ~2125 microns x 2000 microns

Space is allocated.
Reserved space = 2000 x 2500 microns, Area = 5.00 sq mm
Priority time: 26-Nov-79 23:18:09
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>ELLISCT.CIF;2
File creation date: 3-Dec-79 23:42:35
Bounding box = 2000 x 2500 microns, Area = 5.00 sq mm

✔ FuCT

Designer(s): Sai Wai Fu
Description: Square root generator
Est.BB: ~1600 x 1900 microns

Space is allocated.
Reserved space = 1750 x 1626 microns, Area = 2.85 sq mm
Priority time: 1-Dec-79 13:34:10
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>FUCT.CIF;2
File creation date: 3-Dec-79 23:52:32
Bounding box = 1750 x 1626 microns, Area = 2.85 sq mm

✔ GrayCT

Designer(s): Moshe Gray
Description: Array processor
Est.BB: ~1900 x 1900 microns

Design is awaiting allocation.
Required space = 2534 x 2082 microns, Area = 5.28 sq mm
Priority time: 26-Nov-79 23:27:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>GRAYCT.CIF;4
File creation date: 4-Dec-79 15:08:13
Bounding box = 2534 x 2082 microns, Area = 5.28 sq mm

✔ HellerCT

Designer(s): Jack Heller
Description: Digital filter
Est.BB: ~2000 x 2000 microns

Space is allocated.
Reserved space = 2708 x 1326 microns, Area = 3.59 sq mm
Priority time: 26-Nov-79 23:29:12
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HELLERCT.CIF;2
File creation date: 3-Dec-79 23:39:56
Bounding box = 2708 x 1326 microns, Area = 3.59 sq mm

✓ HoCT

Designer(s): Kuo Ting Ho
Description: 10 bit rate multipler
Est.BB: ~1000 x 1700 microns

Design is awaiting allocation.
Required space = 2120 x 1110 microns, Area = 2.35 sq mm
Priority time: 26-Nov-79 23:30:45
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HOCT.CIF;2
File creation date: 3-Dec-79 23:41:41
Bounding box = 2120 x 1110 microns, Area = 2.35 sq mm

✓ KingsleyCT

Designer(s): Chris Kingsley
Description: Serial Multipler
Est.BB: ~2200 microns x 2200 microns

Space is allocated.
Reserved space = 2200 x 2064 microns, Area = 4.54 sq mm
Priority time: 26-Nov-79 23:32:05
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>KINGSLEYCT.CIF;3
File creation date: 4-Dec-79 15:03:33
Bounding box = 2200 x 2064 microns, Area = 4.54 sq mm

✓ LiCT

Designer(s): Peggy Pey-Yun Li
Description: Two's-complement pipeline multiplier
Est.BB: ~1200 x 1700 microns

Space is allocated.
Reserved space = 2176 x 1326 microns, Area = 2.89 sq mm
Priority time: 26-Nov-79 23:33:15
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>LICT.CIF;2
File creation date: 3-Dec-79 23:48:33
Bounding box = 2176 x 1326 microns, Area = 2.89 sq mm

✓ LigockiCT

Designer(s): Terry Ligocki
Description: Scan converter chip
Est.BB: ~2000 X 2000 microns

Design is awaiting allocation.
Required space = 2000 x 4108 microns, Area = 8.22 sq mm
Priority time: 26-Nov-79 23:34:29
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>LIGOCKICT.CIF;3
File creation date: 4-Dec-79 15:11:59
Bounding box = 2000 x 4108 microns, Area = 8.22 sq mm

✓ MostellerCT

Designer(s): Rick Mosteller, Greg Eflan, DIck Lang
Description: Stack-oriented micrprocessor
EstBB: 6000 x 4000 microns

Space is allocated.
Reserved space = 4300 x 2996 microns, Area = 12.88 sq mm
Priority time: 30-Nov-79 17:46:53
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MOSTELLERCT.CIF;3
File creation date: 4-Dec-79 15:09:38
Bounding box = 4300 x 2996 microns, Area = 12.88 sq mm

✓ PapachCT

Designer(s): A.C. Papachristidis
Description: Magnitude comparator
Est.BB: ~2100 x 1200 microns

Space is allocated.
Reserved space = 2000 x 1126 microns, Area = 2.25 sq mm
Priority time: 26-Nov-79 23:41:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PAPACHCT.CIF;2
File creation date: 3-Dec-79 23:29:15
Bounding box = 2000 x 1126 microns, Area = 2.25 sq mm

✓ PedersenCT

Designer(s): Bruce Pedersen
Description: Asynchronous FIFO
Est.BB: ~ 2000 microns x 2000 microns

Design is awaiting allocation.
Required space = 1896 x 2000 microns, Area = 3.79 sq mm
Priority time: 26-Nov-79 23:43:30
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PEDERSENCT.CIF;3
File creation date: 4-Dec-79 15:03:17
Bounding box = 1896 x 2000 microns, Area = 3.79 sq mm

✓ PinesCT

Designer(s): Elliot Pines
Description: Expandable clocking pattern generator chip
Est.BB: ~1800 x 1800 microns

Space is allocated.
Reserved space = 1780 x 1780 microns, Area = 3.17 sq mm
Priority time: 26-Nov-79 23:48:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PINESCT.CIF;2
File creation date: 3-Dec-79 23:34:06
Bounding box = 1780 x 1780 microns, Area = 3.17 sq mm

✓ PursifullCT

Designer(s): Ralph Pursiful
Description: Self-Timed Queue
Est.BB: ~2300 X 2300 microns

Space is allocated.
Reserved space = 1590 x 1590 microns, Area = 2.53 sq mm
Priority time: 27-Nov-79 0:02:06
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PURSIFULLCT.CIF;3
File creation date: 4-Dec-79 15:09:25
Bounding box = 1590 x 1590 microns, Area = 2.53 sq mm

✓ RumphCT HIT

Designer(s): David Rumph
Description: DMA controller
Est.BB: ~2000 x 2000 microns

Design is awaiting allocation.
Required space = 2442 x 2242 microns, Area = 5.47 sq mm
Priority time: 27-Nov-79 17:42:58
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>RUMPHCT.CIF;1
File creation date: 4-Dec-79 13:24:20
Bounding box = 2442 x 2242 microns, Area = 5.47 sq mm

✓ TannerCT

Designer(s): John Tanner and Richard Segal
Description: Single wire interface for a Manipulator (SWIM)
Est.BB: ~3200 x 2200 microns

Space is allocated.
Reserved space = 2000 x 3000 microns, Area = 6.00 sq mm
Priority time: 26-Nov-79 23:57:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>TANNERCT.CIF;3
File creation date: 4-Dec-79 15:06:17
Bounding box = 2000 x 3000 microns, Area = 6.00 sq mm

WalpCT [redacted] → went onto MIT3.

Designer(s): Pat Walp
Description: array processor
Est.BB: ~2200 x 2000 microns

Design is awaiting allocation.
Required space = 2126 x 2050 microns, Area = 4.36 sq mm
Priority time: 3-Dec-79 23:47:47
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WALPCT.CIF;3
File creation date: 4-Dec-79 15:08:49
Bounding box = 2126 x 2050 microns, Area = 4.36 sq mm

✓ WatteyneCT

Designer(s): Thierry Watteyne and Martine Savalle
Description: BCD/binary comparator
Est.BB: ~ 2100 microns x 1600 microns

Space is allocated.
Reserved space = 2100 x 1600 microns, Area = 3.36 sq mm
Priority time: 26-Nov-79 23:59:25
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WATTEYNECT.CIF;2
File creation date: 3-Dec-79 23:44:39
Bounding box = 2100 x 1600 microns, Area = 3.36 sq mm

✓ WhitneyCT

Designer(s): Telle Whitney
Description: Address translator
Est.BB: ~2000 x 2000 microns

Space is allocated.
Reserved space = 1940 x 2126 microns, Area = 4.12 sq mm
Priority time: 27-Nov-79 0:01:04
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WHITNEYCT.CIF;3
File creation date: 4-Dec-79 15:12:25
Bounding box = 1940 x 2126 microns, Area = 4.12 sq mm

CALTECH

Summary of designs from CalTech, updated 4-Dec-79 3:51:33

BartonCT

Designer(s): Eric Barton
Description: LED array driver
Est.BB: ~2125 x 2125 microns

;2

Space is allocated.
Reserved space = 2126 x 2126 microns, Area = 4.52 sq mm
Priority time: 26-Nov-79 22:33:36
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BARTONCT.CIF;2
File creation date: 3-Dec-79 23:33:26
Bounding box = 2126 x 2126 microns, Area = 4.52 sq mm

BozzutoCT

;1

Designer(s): Rick Bozzuto
Description: Pulse width to binary converter
Est.BB: ~1500 x 2300 microns

Space is allocated.
Reserved space = 2120 x 1288 microns, Area = 2.73 sq mm
Priority time: 26-Nov-79 22:35:51
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BOZZUTOCT.CIF;1
File creation date: 3-Dec-79 23:51:28
Bounding box = 2120 x 1288 microns, Area = 2.73 sq mm

CampbellCT

2

Designer(s): James Campbel
Description: Logical processing unit with internal registers
Est.BB: ~1400 X 1400 microns

Space is allocated.
Reserved space = 1856 x 1704 microns, Area = 3.16 sq mm
Priority time: 27-Nov-79 0:03:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>CAMPBELLCT.CIF;2
File creation date: 3-Dec-79 23:38:10
Bounding box = 1856 x 1704 microns, Area = 3.16 sq mm

CocconiCT

;3

Designer: Alan Cocconi
Description: array processor
Est.BB: 2000 x 2000 microns

Space is allocated.
Reserved space = 1896 x 1074 microns, Area = 2.04 sq mm
Priority time: 1-Dec-79 20:20:33
Current submittal is not implementable.
File name: [Maxc]<CALTECH-VLSI>COCCONICT.CIF;2
File creation date: 3-Dec-79 23:25:26

DerbyCT

;4

Designer(s): Howard Derby
Description: Associative Memory
Est.BB: ~2250 x 2250 microns

Design is awaiting allocation.
Required space = 2170 x 2566 microns, Area = 5.57 sq mm
Priority time: 26-Nov-79 22:39:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>DERBYCT.CIF;2
File creation date: 3-Dec-79 23:34:54
Bounding box = 2170 x 2566 microns, Area = 5.57 sq mm

EatonCT

Designer(s): Steve Eaton
Description: Counter/adder
Est.BB: ~ 1400 x 2600 microns

Space is allocated.
Reserved space = 2500 x 1376 microns, Area = 3.44 sq mm
Priority time: 26-Nov-79 23:14:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>EATONCT.CIF;2
File creation date: 3-Dec-79 23:53:13
Bounding box = 2500 x 1376 microns, Area = 3.44 sq mm

EllisCT

Designer(s): Mike Ellis
Description: Stepping motor controller
Est.BB: ~2125 microns x 2000 microns

Space is allocated.
Reserved space = 2000 x 2500 microns, Area = 5.00 sq mm
Priority time: 26-Nov-79 23:18:09
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>ELLISCT.CIF;2
File creation date: 3-Dec-79 23:42:35
Bounding box = 2000 x 2500 microns, Area = 5.00 sq mm

FuCT

Designer(s): Sai Wai Fu
Description: Square root generator
Est.BB: ~1600 x 1900 microns

Space is allocated.
Reserved space = 1750 x 1626 microns, Area = 2.85 sq mm
Priority time: 1-Dec-79 13:34:10
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>FUCT.CIF;2
File creation date: 3-Dec-79 23:52:32
Bounding box = 1750 x 1626 microns, Area = 2.85 sq mm

GrayCT

Designer(s): Moshe Gray
Description: Array processor
Est.BB: ~1900 x 1900 microns

Design is awaiting allocation.
Required space = 2534 x 2152 microns, Area = 5.45 sq mm
Priority time: 26-Nov-79 23:27:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>GRAYCT.CIF;2
File creation date: 3-Dec-79 23:43:51
Bounding box = 2534 x 2152 microns, Area = 5.45 sq mm

HellerCT

Designer(s): Jack Heller
Description: Digital filter
Est.BB: ~2000 x 2000 microns

Space is allocated.
Reserved space = 2708 x 1326 microns, Area = 3.59 sq mm
Priority time: 26-Nov-79 23:29:12
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HELLERCT.CIF;2
File creation date: 3-Dec-79 23:39:56
Bounding box = 2708 x 1326 microns, Area = 3.59 sq mm

HoCT

Designer(s): Kuo Ting Ho
Description: 10 bit rate multipler
Est.BB: ~1000 x 1700 microns

Design is awaiting allocation.
Required space = 2120 x 1110 microns, Area = 2.35 sq mm
Priority time: 26-Nov-79 23:30:45
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HOCT.CIF;2
File creation date: 3-Dec-79 23:41:41
Bounding box = 2120 x 1110 microns, Area = 2.35 sq mm

KingsleyCT

Designer(s): Chris Kingsley
Description: Serial Multipler
Est.BB: ~2200 microns x 2200 microns

Space is allocated.
Reserved space = 2200 x 2200 microns, Area = 4.84 sq mm
Priority time: 26-Nov-79 23:32:05
Current submittal is not implementable.
File name: [Maxc]<CALTECH-VLSI>KINGSLEYCT.CIF;2
File creation date: 3-Dec-79 23:31:16

LiCT

Designer(s): Peggy Pey-Yun Li
Description: Two's-complement pipeline multiplier
Est.BB: ~1200 x 1700 microns

Space is allocated.
Reserved space = 2176 x 1326 microns, Area = 2.89 sq mm
Priority time: 26-Nov-79 23:33:15
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>LICT.CIF;2
File creation date: 3-Dec-79 23:48:33
Bounding box = 2176 x 1326 microns, Area = 2.89 sq mm

LigockiCT

Designer(s): Terry Ligocki
Description: Scan converter chip
Est.BB: ~2000 X 2000 microns

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm
Priority time: 26-Nov-79 23:34:29
Current submittal is not implementable.
File name: [Maxc]<CALTECH-VLSI>LIGOCKICT.CIF;2
File creation date: 3-Dec-79 23:53:54

MartinCT

Designer(s): Kreg Martin
Description: Serial Array processing element
Est.BB: ~2000 x 2375 microns

Design is awaiting allocation.
Required space = 2376 x 2126 microns, Area = 5.05 sq mm
Priority time: 1-Dec-79 18:49:01
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MARTINCT.CIF;2
File creation date: 3-Dec-79 23:40:55
Bounding box = 2376 x 2126 microns, Area = 5.05 sq mm

MeadorCT

Designer(s): Jim Meador
Description: 4-digit clock chip
Est.BB: ~2100 x 1800 microns

Space is allocated.
Reserved space = 2000 x 2388 microns, Area = 4.78 sq mm
Priority time: 1-Dec-79 20:29:19
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MEADORCT.CIF;4
File creation date: 1-Dec-79 20:29:19
Bounding box = 2000 x 2388 microns, Area = 4.78 sq mm

MostellerCT

Designer(s): Rick Mosteller, Greg Eflan, DIck Lang
Description: Stack-oriented micrprocessor
EstBB: 6000 x 4000 microns

Space is allocated.
Reserved space = 4300 x 2996 microns, Area = 12.88 sq mm
Priority time: 30-Nov-79 17:46:53
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MOSTELLERCT.CIF;2
File creation date: 3-Dec-79 23:50:32
Bounding box = 4300 x 2996 microns, Area = 12.88 sq mm

PapachCT

Designer(s): A.C. Papachristidis
Description: Magnitude comparator
Est.BB: ~2100 x 1200 microns

Space is allocated.
Reserved space = 2000 x 1126 microns, Area = 2.25 sq mm
Priority time: 26-Nov-79 23:41:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PAPACHCT.CIF;2
File creation date: 3-Dec-79 23:29:15
Bounding box = 2000 x 1126 microns, Area = 2.25 sq mm

PedersenCT

Designer(s): Bruce Pedersen
Description: Asynchronous FIFO
Est.BB: ~ 2000 microns x 2000 microns

Design is awaiting allocation.
Required space = 1896 x 2000 microns, Area = 3.79 sq mm
Priority time: 26-Nov-79 23:43:30
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PEDERSENCT.CIF;2
File creation date: 3-Dec-79 23:30:23
Bounding box = 1896 x 2000 microns, Area = 3.79 sq mm

PinesCT

Designer(s): Elliot Pines
Description: Expandable clocking pattern generator chip
Est.BB: ~1800 x 1800 microns

Space is allocated.
Reserved space = 1780 x 1780 microns, Area = 3.17 sq mm
Priority time: 26-Nov-79 23:48:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PINESCT.CIF;2
File creation date: 3-Dec-79 23:34:06
Bounding box = 1780 x 1780 microns, Area = 3.17 sq mm

PursifullCT

Designer(s): Ralph Pursiful
Description: Self-Timed Queue
Est.BB: ~2300 X 2300 microns

Space is allocated.
Reserved space = 1590 x 1590 microns, Area = 2.53 sq mm
Priority time: 27-Nov-79 0:02:06
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PURSIFULLCT.CIF;2
File creation date: 3-Dec-79 23:49:37
Bounding box = 1590 x 1590 microns, Area = 2.53 sq mm

RumphCT

Designer(s): David Rumph
Description: DMA controller
Est.BB: ~2000 x 2000 microns

;1

Design is not ready for space allocation.
Current submittal checked ok.
File name: [Maxc]<CALTECH-VLSI>RUMPHCT.CIF;1
File creation date: 27-Nov-79 17:42:58
Bounding box = 1002 x 1130 microns, Area = 1.13 sq mm

ShahCT

~~Designer(s): Deepak Shah~~
~~Description: Array processor~~
~~Est.BB: ~2250 x 2250 microns~~

DEL

Space is allocated.
Reserved space = 2250 x 2250 microns, Area = 5.06 sq mm
Priority time: 26-Nov-79 23:50:18
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>SHAHCT.CIF;2
File creation date: 3-Dec-79 23:32:11
Bounding box = 2250 x 2250 microns, Area = 5.06 sq mm

TannerCT

Designer(s): John Tanner and Richard Segal
Description: Single wire interface for a Manipulator (SWIM)
Est.BB: ~3200 x 2200 microns

;3

Space is allocated.
Reserved space = 2000 x 3000 microns, Area = 6.00 sq mm
Priority time: 26-Nov-79 23:57:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>TANNERCT.CIF;2
File creation date: 3-Dec-79 23:39:02
Bounding box = 2000 x 3000 microns, Area = 6.00 sq mm

WalpCT

Designer(s): Pat Walp
Description: array processor
Est.BB: ~2200 x 2000 microns

;3

Design is awaiting allocation.
Required space = 2126 x 2050 microns, Area = 4.36 sq mm
Priority time: 3-Dec-79 23:47:47
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WALPCT.CIF;2
File creation date: 3-Dec-79 23:47:47
Bounding box = 2126 x 2050 microns, Area = 4.36 sq mm

WatteyneCT

Designer(s): Thierry Watteyne and Martine Savalle
Description: BCD/binary comparator
Est.BB: ~ 2100 microns x 1600 microns

;2

Space is allocated.
Reserved space = 2100 x 1600 microns, Area = 3.36 sq mm
Priority time: 26-Nov-79 23:59:25
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WATTEYNECT.CIF;2
File creation date: 3-Dec-79 23:44:39
Bounding box = 2100 x 1600 microns, Area = 3.36 sq mm

WhitneyCT

Designer(s): Telle Whitney
Description: Address translator
Est.BB: ~2000 x 2000 microns

13

Space is allocated.
Reserved space = 1940 x 2126 microns, Area = 4.12 sq mm
Priority time: 27-Nov-79 0:01:04
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WHITNEYCT.CIF;2
File creation date: 3-Dec-79 23:54:52
Bounding box = 1940 x 2126 microns, Area = 4.12 sq mm

CALTECH PRIORITIES

(1) Mosteller, Tanner, Whitney, Barton
Derby, Li, Ligocki

(2) (all the rest)

(3) ? Cocconi ?

---

(4) Walp, Meador, Rumph

↓ HIT

Memo from: LYNN CONWAY

CMU SUMMARY

5 proj.	28.10 mm^2

XEROX

CMU FINAL

Summary of designs from CMU, updated 4-Dec-79 22:28:11

EbelingCMU

Designer: Carl Ebeling
Description: Rebound Sorter
Est.BB: 2000 X 2000 microns

Space is allocated.
Reserved space = 1856 x 1856 microns, Area = 3.44 sq mm
Priority time: 27-Nov-79 8:04:24
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>EBELINGCMU.CIF;2
File creation date: 4-Dec-79 8:15:59
Bounding box = 1856 x 1856 microns, Area = 3.44 sq mm

GuptaCMU

Designer: Satish Gupta
Description: Video Buffer
Est.BB: 5000 X 1000 microns

Space is allocated.
Reserved space = 1006 x 5668 microns, Area = 5.70 sq mm
Priority time: 27-Nov-79 17:22:44
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>GUPTACMU.CIF;2
File creation date: 1-Dec-79 13:53:57
Bounding box = 1006 x 5668 microns, Area = 5.70 sq mm

HoeyCMU

Designer: Dan Hoey
Description: Experimental Adder
EstBB: 4000 x 4000 microns

Space is allocated.
Reserved space = 1188 x 1976 microns, Area = 2.35 sq mm
Priority time: 27-Nov-79 17:23:54
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>HOEYCMU.CIF;4
File creation date: 3-Dec-79 9:36:41
Bounding box = 1188 x 1976 microns, Area = 2.35 sq mm

KungCMU

Designer: H. T. Kung, S. W. Song
Description: Image Processing Chip
Est.BB: 3500 X 2300 microns

Design is awaiting allocation.
Required space = 4160 x 2948 microns, Area = 12.26 sq mm
Priority time: 1-Dec-79 11:29:02
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>KUNGCMU.CIF;8
File creation date: 4-Dec-79 21:28:30
Bounding box = 4160 x 2948 microns, Area = 12.26 sq mm

SongCMU

Designer: Siang W Song
Description: A small database machine
Est.BB: 2000 X 2000 microns

Space is allocated.
Reserved space = 2224 x 1954 microns, Area = 4.35 sq mm
Priority time: 27-Nov-79 8:54:16
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>SONGCMU.CIF;5

File creation date: 4-Dec-79 15:05:14
Bounding box = 2224 x 1954 microns, Area = 4.35 sq mm

Memo from: LYNN CONWAY

ILLINOIS SUMMARY

5 proj.	38.91 mm^2

XEROX

ILLINOIS FINAL

Summary of designs from Illinois, updated 4-Dec-79 20:40:30

✓ AdrianUI

Designers: Frank Adrian, Nick Fiduccia, Bud Pflug
Description: Functional equivalent of AMD 2901 ALU to compare MOS, TTL
Est.BB: ~ 2000 X 2000 microns

Space is allocated.
Reserved space = 2710 x 4388 microns, Area = 11.89 sq mm
Priority time: 27-Nov-79 15:23:08
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>ADRIANUI.CIF;3
File creation date: 4-Dec-79 13:24:09
Bounding box = 2710 x 4388 microns, Area = 11.89 sq mm

✓ ClassUI

Designers: Class
Description: Twos complement 4 x 4 array multiplier
Est.BB: 1200 x 1200

Space is allocated.
Reserved space = 1714 x 1498 microns, Area = 2.57 sq mm
Priority time: 27-Nov-79 11:36:20
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>CLASSUI.CIF;3
File creation date: 3-Dec-79 13:54:59
Bounding box = 1714 x 1498 microns, Area = 2.57 sq mm

✓ HanesUI

Designers: Larry Hanes, Dave Yen
Description: Twos complement array divider
Est.BB: ~ 2000 X 2000 microns

Space is allocated.
Reserved space = 2616 x 2636 microns, Area = 6.90 sq mm
Priority time: 27-Nov-79 15:00:02
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>HANESUI.CIF;3
File creation date: 3-Dec-79 21:33:23
Bounding box = 2616 x 2636 microns, Area = 6.90 sq mm

✓ LuhukayUI

Designer: Joe Luhukay
Description: Pipelined multiplier, registers also used for testability
Est.BB: ~ 2000 X 1250 microns

Design is awaiting allocation.
Required space = 2572 x 4140 microns, Area = 10.65 sq mm
Priority time: 22-Nov-79 21:26:35
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>LUHUKAYUI.CIF;3
File creation date: 4-Dec-79 7:21:44
Bounding box = 2572 x 4140 microns, Area = 10.65 sq mm

✓ MontoyeUI

Designers: Bob Montoye, Al Casavant
Description: Carry lookahead adder (soln. proposed by Gajski and Kung)
Est.BB: ~ 2000 X 1500 microns.

Design is awaiting allocation.
Required space = 2628 x 2626 microns, Area = 6.90 sq mm
Priority time: 27-Nov-79 8:33:59
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>MONTOYEUI.CIF;2
File creation date: 4-Dec-79 13:28:21
Bounding box = 2628 x 2626 microns, Area = 6.90 sq mm

Memo from: LYNN CONWAY

MIT

SUMMARY:

~~15~~ 14 proj.	91.23 mm²

XEROX

MIT FINAL

Summary of designs from MIT, updated 4-Dec-79 19:02:23

✓AllenMIT

Designers: Don Allen, Jerry Burchfiel
Description: Variable Length Field Decoder
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2218 x 2484 microns, Area = 5.51 sq mm
Priority time: 28-Nov-79 7:45:20
Current submittal is acceptable for implementation.
File name: [Maxc]<ABELL>ALLENMIT.CIF;3
File creation date: 4-Dec-79 18:44:50
Bounding box = 2218 x 2484 microns, Area = 5.51 sq mm

✓BataliMIT

Designers: John Batali
Description: Zero-Crossing Detector for Image Processing
Est.BB 2650 x 1575

Design is awaiting allocation.
Required space = 2644 x 1738 microns, Area = 4.60 sq mm
Priority time: 29-Nov-79 5:59:14
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>BATALIMIT.CIF;3
File creation date: 4-Dec-79 16:35:08
Bounding box = 2644 x 1738 microns, Area = 4.60 sq mm

BodonyMIT

Designers: Larry Bodony, Bruce Rose
Description: Logic State Analyzer
Est.BB: 4500 x 2650 microns

Design is awaiting allocation.
Required space = 4500 x 4336 microns, Area = 19.51 sq mm
Priority time: 28-Nov-79 7:45:43
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>BODONYMIT.CIF;2
File creation date: 4-Dec-79 16:55:27
Bounding box = 4500 x 4336 microns, Area = 19.51 sq mm

ChangMIT

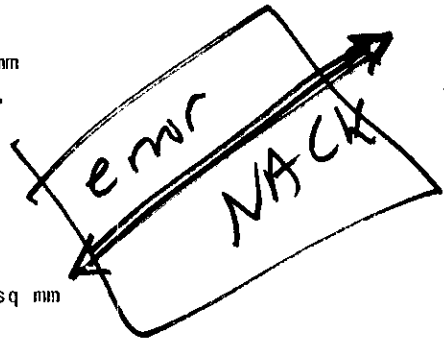
Designers: Frank Chang, Doug Williams
Description: Error-detecting block transfer oriented channel interface
Est.BB: 2500 x 5250 microns

Space is allocated.
Reserved space = 2764 x 2500 microns, Area = 6.91 sq mm
Priority time: 29-Nov-79 5:59:33
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>CHANGMIT.CIF;4
File creation date: 4-Dec-79 16:17:37
Bounding box = 2764 x 2500 microns, Area = 6.91 sq mm

✓ChuMIT

Designers: Tam-Anh Chu, Nhi-Anh Chu, Steve McCormick
Description: Second order digital filter stage
Est.BB: 2400 x 6200 microns

Space is allocated.
Reserved space = 6146 x 2278 microns, Area = 14.00 sq mm
Priority time: 29-Nov-79 6:00:45
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>CHUMIT.CIF;3
File creation date: 4-Dec-79 13:47:06
Bounding box = 6146 x 2278 microns, Area = 14.00 sq mm



RANDY SAYS THIS CAN'T BE RIGHT (TOO BIG!)

? TRY TO LOOK AT THIS

FichtenbaumMIT

Designers:Matt Fichtenbaum
Description: A digital pulse rate monitor
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm
Priority time: 29-Nov-79 15:05:20
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>FICHTENBAUMMIT.CIF;2
File creation date: 4-Dec-79 14:07:50
Bounding box = 2500 x 2500 microns, Area = 6.25 sq mm

GoddeauMIT

Designers:David Goddeau, Jonathan Sieber, Chris Terman
Description: A first-in, priority-out buffer
Est.BB:3000 x 3000 microns

Space is allocated.
Reserved space = 2928 x 2954 microns, Area = 8.65 sq mm
Priority time: 28-Nov-79 15:16:15
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GODDEAUMIT.CIF;2
File creation date: 4-Dec-79 0:07:02
Bounding box = 2928 x 2954 microns, Area = 8.65 sq mm

GoodrichMIT

Designers: Earl Goodrich
Description: CRT controller
Est.BB: 2000 x 1600 microns

Space is allocated.
Reserved space = 1856 x 1520 microns, Area = 2.82 sq mm
Priority time: 1-Dec-79 20:52:01
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GOODRICHMIT.CIF;2
File creation date: 4-Dec-79 12:49:03
Bounding box = 1856 x 1520 microns, Area = 2.82 sq mm

GramlichMIT

Designers: Wayne Gramlich, Carl Seaquist
Description: A writable PLA in which the programming of the AND and
OR planes is defined by contents of the static RAM cells.
Also cam program feedback loops to form finite state machines.
Est.BB: 2200 X 1700 microns.

Design is awaiting allocation.
Required space = 1524 x 1906 microns, Area = 2.90 sq mm
Priority time: 27-Nov-79 10:13:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GRAMLICHMIT.CIF;2
File creation date: 29-Nov-79 19:35:37
Bounding box = 1524 x 1906 microns, Area = 2.90 sq mm

GrondalskiMIT

Designers: Robert Grondalski
Description: Writeable PLA
Est.BB: 2200 x 2200 microns

Space is allocated.
Reserved space = 2200 x 2200 microns, Area = 4.84 sq mm
Priority time: 28-Nov-79 7:47:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GRONDALSKIMIT.CIF;2
File creation date: 4-Dec-79 13:27:20

Bounding box = 2200 x 2200 microns, Area = 4.84 sq mm

✔HamiltonMIT

Designers:Brian Hamilton
Description: Digital Alarm Clock
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm
Priority time: 1-Dec-79 11:25:05
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>HAMILTONMIT.CIF;2
File creation date: 4-Dec-79 16:18:21
Bounding box = 2500 x 2500 microns, Area = 6.25 sq mm

✔KathailMIT

Designers: Vinod Kathail, Keshav Pingali
Description: an interpreter for mapping programs onto a data flow computer
Est.BB: 2250 x 1750 microns

Design is awaiting allocation.
Required space = 1590 x 2228 microns, Area = 3.54 sq mm
Priority time: 29-Nov-79 6:01:43
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>KATHAILMIT.CIF;3
File creation date: 4-Dec-79 15:28:28
Bounding box = 1590 x 2228 microns, Area = 3.54 sq mm

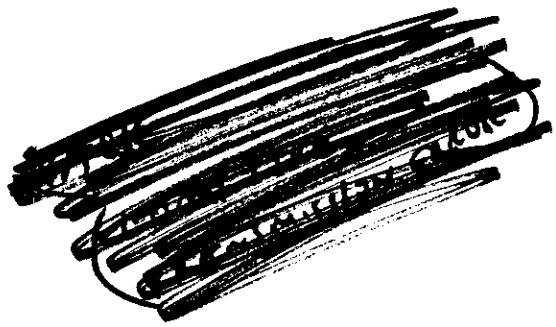
✔KhouryMIT

Designers: John Khoury
Description: Up-Down counter with programmable modulus
Est.BB: 2000 x 1725 microns

Space is allocated.
Reserved space = 2000 x 1726 microns, Area = 3.45 sq mm
Priority time: 29-Nov-79 15:06:27
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>KHOURYMIT.CIF;2
File creation date: 4-Dec-79 13:26:17
Bounding box = 2000 x 1726 microns, Area = 3.45 sq mm

✔PasemanMIT

Designers: Bill Paseman
Description: Music Synthesizer
Est.BB:4250 x 1750 microns



Space is allocated.
Reserved space = 4438 x 2944 microns, Area = 13.07 sq mm
Priority time: 30-Nov-79 13:07:25
Current submittal is not implementable.
File name: [Maxc]<MIT-VLSI>PASEMANMIT.CIF;2
File creation date: 4-Dec-79 10:17:59

✔PicardMIT

Designers: Len Picard
Description: Variable format field extractor and compactor
Est.BB: 2000 x 1750 microns

Space is allocated.
Reserved space = 2000 x 1688 microns, Area = 3.38 sq mm
Priority time: 29-Nov-79 6:02:08
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>PICARDMIT.CIF;3
File creation date: 4-Dec-79 12:50:38
Bounding box = 2000 x 1688 microns, Area = 3.38 sq mm

RivestMIT

Designers: Ron Rivest, Len Adleman, Adi Shamir
Description: Section of a Multiplier
Est.BB: 2000 x 2000

Space is allocated.
Reserved space = 2250 x 2250 microns, Area = 5.06 sq mm
Priority time: 29-Nov-79 6:02:47
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>RIVESTMIT.CIF;5
File creation date: 3-Dec-79 19:40:08
Bounding box = 2250 x 2250 microns, Area = 5.06 sq mm

M.I.T. Priorities

ONLY ONE TO QUESTION IS Chang.
IF IT LINES UP OK, DO IT.

TRY TO FIX PASEMAN.

RANDY WILL RETRANSMIT ✓ DONE O.K.

MIT

Summary of designs from MIT, updated 4-Dec-79 3:51:33

Latest scoop from REB @ 4:45

AllenMIT

Designers: Don Allen, Jerry Burchfiel
Description: Variable Length Field Decoder
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2484 x 2218 microns, Area = 5.51 sq mm
Priority time: 28-Nov-79 7:45:20
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>ALLENMIT.CIF;1
File creation date: 28-Nov-79 7:45:20
Bounding box = 2484 x 2218 microns, Area = 5.51 sq mm

;2

BataliMIT

Designers: John Batali
Description: Zero-Crossing Detector for Image Processing
Est.BB 2650 x 1575

Space is allocated.
Reserved space = 2626 x 1626 microns, Area = 4.27 sq mm
Priority time: 29-Nov-79 5:59:14
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>BATALIMIT.CIF;2
File creation date: 29-Nov-79 5:59:14
Bounding box = 2626 x 1626 microns, Area = 4.27 sq mm

;3

BodonyMIT

Designers: Larry Bodony, Bruce Rose
Description: Logic State Analyzer
Est.BB: 4500 x 2650 microns

Space is allocated.
Reserved space = 924 x 944 microns, Area = 0.87 sq mm
Priority time: 28-Nov-79 7:45:43
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>BODONYMIT.CIF;1
File creation date: 28-Nov-79 7:45:43
Bounding box = 924 x 944 microns, Area = 0.87 sq mm

probable? (check recent mail)

ChangMIT

Designers: Frank Chang, Doug Williams
Description: Error-detecting block transfer oriented channel interface
Est.BB: 2500 x 5250 microns

Space is allocated.
Reserved space = 5250 x 2500 microns, Area = 13.13 sq mm
Priority time: 29-Nov-79 5:59:33
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>CHANGMIT.CIF;2
File creation date: 29-Nov-79 5:59:33
Bounding box = 5250 x 2500 microns, Area = 13.13 sq mm

;4

ChuMIT

Designers: Tam-Anh Chu, Nhi-Anh Chu, Steve McCormick
Description: Second order digital filter stage
Est.BB: 2400 x 6200 microns

Space is allocated.
Reserved space = 6146 x 2296 microns, Area = 14.11 sq mm
Priority time: 29-Nov-79 6:00:45
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>CHUMIT.CIF;2
File creation date: 29-Nov-79 6:00:45
Bounding box = 6146 x 2296 microns, Area = 14.11 sq mm

;3

FichtenbaumMIT

Designers:Matt Fichtenbaum
Description: A digital pulse rate monitor
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm
Priority time: 29-Nov-79 15:05:20
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>FICHTENBAUMMIT.CIF;1
File creation date: 29-Nov-79 15:05:20
Bounding box = 2500 x 2500 microns, Area = 6.25 sq mm

~~GandlerMIT~~

Designers: William Gandler
Description: Controller for 4 phase motor
Est.BB: 2000 x 2000 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

GoddeauMIT

Designers:David Goddeau, Jonathan Sieber, Chris Terman
Description: A first-in, priority-out buffer
Est.BB:3000 x 3000 microns

Space is allocated.
Reserved space = 2928 x 2954 microns, Area = 8.65 sq mm
Priority time: 28-Nov-79 15:16:15
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GODDEAUMIT.CIF;2
File creation date: 4-Dec-79 0:07:02
Bounding box = 2928 x 2954 microns, Area = 8.65 sq mm

GoodrichMIT

Designers: Earl Goodrich
Description: CRT controller
Est.BB: 2000 x 1600 microns

Space is allocated.
Reserved space = 1862 x 1546 microns, Area = 2.88 sq mm
Priority time: 1-Dec-79 20:52:01
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GOODRICHMIT.CIF;1
File creation date: 1-Dec-79 20:52:01
Bounding box = 1862 x 1546 microns, Area = 2.88 sq mm

GramlichMIT

Designers: Wayne Gramlich, Carl Seaquist
Description: A writable PLA in which the programming of the AND and
OR planes is defined by contents of the static RAM cells.
Also cam program feedback loops to form finite state machines.
Est.BB: 2200 X 1700 microns.

Design is awaiting allocation.
Required space = 1524 x 1906 microns, Area = 2.90 sq mm
Priority time: 27-Nov-79 10:13:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GRAMLICHMIT.CIF;2
File creation date: 29-Nov-79 19:35:37
Bounding box = 1524 x 1906 microns, Area = 2.90 sq mm

GrondalskiMIT

Designers: Robert Grondalski
Description: Writeable PLA
Est.BB: 2200 x 2200 microns

Space is allocated.
Reserved space = 2200 x 2200 microns, Area = 4.84 sq mm
Priority time: 28-Nov-79 7:47:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GRONDALSKIMIT.CIF;1
File creation date: 28-Nov-79 7:47:36
Bounding box = 2200 x 2200 microns, Area = 4.84 sq mm

HamiltonMIT

j2

Designers:Brian Hamilton
Description: Digital Alarm Clock
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm
Priority time: 1-Dec-79 11:25:05
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>HAMILTONMIT.CIF;1
File creation date: 1-Dec-79 11:25:05
Bounding box = 2500 x 2500 microns, Area = 6.25 sq mm

~~JangMIT~~ delete

Designers: Saquib Jang
Description: Priority storage system
Est.BB: 2500 x 1400 microns

Design is not ready for space allocation.
Current submittal is not implementable.
File name: [Maxc]<MIT-VLSI>JANGMIT.CIF;1
File creation date: 28-Nov-79 7:47:59

KathailMIT

j3

Designers: Vinod Kathail, Keshav Pingali
Description: an interpreter for mapping programs onto a data flow computer
Est.BB: 2250 x 1750 microns

Space is allocated.
Reserved space = 904 x 1168 microns, Area = 1.06 sq mm
Priority time: 29-Nov-79 6:01:43
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>KATHAILMIT.CIF;2
File creation date: 29-Nov-79 6:01:43
Bounding box = 904 x 1168 microns, Area = 1.06 sq mm

KhouryMIT

j2

Designers: John Khoury
Description: Up-Down counter with programmable modulus
Est.BB: 2000 x 1725 microns

Space is allocated.
Reserved space = 2000 x 1726 microns, Area = 3.45 sq mm
Priority time: 29-Nov-79 15:06:27
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>KHOURYMIT.CIF;1
File creation date: 29-Nov-79 15:06:27
Bounding box = 2000 x 1726 microns, Area = 3.45 sq mm

MayleMIT

delete

(~~probably won't make it~~)

Designers: Neil Mayle
Description: Crossbar for AI inference networks
Est.BB: 2000 x 2000 microns

Design is awaiting allocation.
Required space = 2250 x 2126 microns, Area = 4.78 sq mm
Priority time: 30-Nov-79 12:04:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>MAYLEMIT.CIF;2
File creation date: 3-Dec-79 10:45:41
Bounding box = 2250 x 2126 microns, Area = 4.78 sq mm

PasemanMIT ;2

Designers: Bill Paseman
Description: Music Synthesizer
Est.BB:4250 x 1750 microns

Space is allocated.
Reserved space = 4438 x 2944 microns, Area = 13.07 sq mm
Priority time: 30-Nov-79 13:07:25
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>PASEMANMIT.CIF;1
File creation date: 30-Nov-79 13:07:25
Bounding box = 4438 x 2944 microns, Area = 13.07 sq mm

PicardMIT ;3

Designers: Len Picard
Description: Variable format field extractor and compactor
Est.BB: 2000 x 1750 microns

Space is allocated.
Reserved space = 2000 x 1688 microns, Area = 3.38 sq mm
Priority time: 29-Nov-79 6:02:08
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>PICARDMIT.CIF;2
File creation date: 29-Nov-79 6:02:08
Bounding box = 2000 x 1688 microns, Area = 3.38 sq mm

[redacted] delete

Designers: Andrew Ressler, Carl Hewitt, Phyliss Koton
Description: communications chip for interconnecting processors
in a multiple processor system
Est.BB: 4500 x 5200 microns

Space is allocated.
Reserved space = 5000 x 5898 microns, Area = 29.49 sq mm
Priority time: 1-Dec-79 20:52:33
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>RESSLERMIT.CIF;2
File creation date: 1-Dec-79 20:52:33
Bounding box = 5000 x 5898 microns, Area = 29.49 sq mm

RiesMIT ? delete (probably want to do it)

Designers: Paul Ries
Description: Dual rail, self-timed FIFO, arbiter test circuits
Est.BB: 2000 x 2000 microns

Space is allocated.
Reserved space = 1720 x 1096 microns, Area = 1.89 sq mm
Priority time: 29-Nov-79 6:02:30
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>RIESMIT.CIF;2
File creation date: 29-Nov-79 6:02:30
Bounding box = 1720 x 1096 microns, Area = 1.89 sq mm

RivestMIT ;5

Designers: Ron Rivest, Len Adleman, Adi Shamir
Description: Section of a Multiplier
Est.BB: 2000 x 2000

```
Space is allocated.
Reserved space = 2250 x 2250 microns, Area = 5.06 sq mm
Priority time: 29-Nov-79  6:02:47
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>RIVESTMIT.CIF;5
File creation date:  3-Dec-79 19:40:08
Bounding box = 2250 x 2250 microns, Area = 5.06 sq mm
----------------------------------------
```

OTHER SUMMARY

6 proj.	65.50 mm^2

(Doc chips not counted)

OTHER FINAL

Summary of designs from Other, updated 4-Dec-79 20:40:30

BoydOT

Delete

Designer: David Boyd

Design is not ready for space allocation.
No file has been submitted for implementation.

GlasserOT

Designer: Lance Glasser

Design is awaiting allocation.
Required space = 1486 x 808 microns, Area = 1.20 sq mm
Priority time: 1-Dec-79 13:31:38
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>GLASSEROT.CIF;1
File creation date: 1-Dec-79 13:31:38
Bounding box = 1486 x 808 microns, Area = 1.20 sq mm

KehlOT

Designer: Ted Kehl, Ram Rao, Ed Lazowska
Description: Address intercept logic for microcomputer
Est.BB: 1815 X 1780 microns

Design is awaiting allocation.
Required space = 1818 x 1782 microns, Area = 3.24 sq mm
Priority time: 24-Nov-79 12:28:02
Current submittal is acceptable for implementation.
File name: [maxc]<LYON>KEHLOT.CIF;1
File creation date: 24-Nov-79 12:28:02
Bounding box = 1818 x 1782 microns, Area = 3.24 sq mm

LhDoc1

This is the left half of the document chip

Space is allocated.
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm
Priority time: 2-Dec-79 22:04:51
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>LHCHIP.CIF;1
File creation date: 2-Dec-79 22:04:51
Bounding box = 2918 x 4688 microns, Area = 13.68 sq mm

LhDoc2

This is the left half of the document chip

Space is allocated.
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm
Priority time: 2-Dec-79 22:04:51
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>LHCHIP.CIF;1
File creation date: 2-Dec-79 22:04:51
Bounding box = 2918 x 4688 microns, Area = 13.68 sq mm

MurrayOT

Designer: John Murray

Design is awaiting allocation.
Required space = 1512 x 1642 microns, Area = 2.48 sq mm
Priority time: 3-Dec-79 11:40:27
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>MURRAYOT.CIF;1
File creation date: 3-Dec-79 11:40:27
Bounding box = 1512 x 1642 microns, Area = 2.48 sq mm

RHDoc1

This is the right side document chip

Space is allocated.
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm
Priority time: 2-Dec-79 22:10:48
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>RHCHIP.CIF;1
File creation date: 2-Dec-79 22:10:48
Bounding box = 3548 x 4424 microns, Area = 15.70 sq mm

RHDoc2

This is the right side document chip

Space is allocated.
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm
Priority time: 2-Dec-79 22:10:48
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>RHCHIP.CIF;1
File creation date: 2-Dec-79 22:10:48
Bounding box = 3548 x 4424 microns, Area = 15.70 sq mm

RodgersOT

Designer: Mike Rodgers

Design is awaiting allocation.
Required space = 1248 x 1708 microns, Area = 2.13 sq mm
Priority time: 3-Dec-79 13:12:01
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>RODGERSOT.CIF;3
File creation date: 3-Dec-79 13:12:01
Bounding box = 1248 x 1708 microns, Area = 2.13 sq mm

Schip2

Designers: Gerry Sussman, Jack Holloway, Guy Steele, Alan Bell
Description: Lisp Microprocesser
Est.BB: 7548 X 5925 microns

ITERATE

Space is allocated.
Reserved space = 5926 x 7548 microns, Area = 44.73 sq mm
Priority time: 19-Nov-79 21:25:06
Current submittal is acceptable for implementation.
File name: [Maxc1]<ABELL>SCHIP2C.CIF;1
File creation date: 19-Nov-79 21:26:06
Bounding box = 5926 x 7548 microns, Area = 44.73 sq mm

SmithOT

Designer(s): Lee Smith, Irene Buchanan
Description: Link design
Est.BB: ~ 2000 X 1400 microns.

Delete

Design is not ready for space allocation.
No file has been submitted for implementation.

SynderOT

Designer: Larry Synder (of Yale, now at U. Wash.)
Description: A binary tree processor that computes boolean functions, with inputs at the leaves and at the root.
Est.BB: 3420 x 3470 microns

Design is awaiting allocation.
Required space = 3418 x 3430 microns, Area = 11.72 sq mm
Priority time: 27-Nov-79 18:49:56

```
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>SNYDEROT.CIF;1
File creation date:  3-Dec-79 11:23:20
Bounding box = 3418 x 3430 microns, Area = 11.72 sq mm
----------------------------------------
```

Memo from: LYNN CONWAY

U of R Summary

5 proj.	30.34 mm^2

XEROX

UofR FINAL

Summary of designs from UofR, updated 4-Dec-79 23:13:17

✔ KedemUR

Designers(s): Gershon Kedem and Michel Denber
Description: Infinite precision multiplier
Est.BB: ~ 2000 x 2000 microns.

Design is awaiting allocation.
Required space = 2698 x 2786 microns, Area = 7.52 sq mm
Priority time: 4-Dec-79 20:06:31
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>KEDEMUR.CIF;1
File creation date: 4-Dec-79 20:06:31
Bounding box = 2698 x 2786 microns, Area = 7.52 sq mm

✔ LyonsUR

Implementer: Bob Lyons
Description: Programmable Frequency Generator
Est.BB: 3000 microns x 3000 microns

Design is awaiting allocation.
Required space = 2748 x 2276 microns, Area = 6.25 sq mm
Priority time: 4-Dec-79 20:04:24
Current submittal is acceptable for implementation.
File name: [Maxc]<UOFR-VLSI>LYONSUR.CIF;2
File creation date: 4-Dec-79 20:04:24
Bounding box = 2748 x 2276 microns, Area = 6.25 sq mm

✔ SohmUR

Designers: Larry Sohm, Pat Chan, Bill Notowitz
Description: Digital Phase lock loop
Est.BB: 1500 x 3000 microns.

Design is awaiting allocation.
Required space = 3610 x 2634 microns, Area = 9.51 sq mm
Priority time: 4-Dec-79 19:06:24
Current submittal is acceptable for implementation.
File name: [Maxc]<UOFR-VLSI>SOHMUR.CIF;2
File creation date: 4-Dec-79 19:06:24
Bounding box = 3610 x 2634 microns, Area = 9.51 sq mm

✔ TiloveUR

Designer(s): Bob Tilove, Jarek Rossignac
Description: This is a bit slice coordinate transformer
Est. BB: ~ 1400 X 2000 microns.

Design is awaiting allocation.
Required space = 1934 x 1326 microns, Area = 2.56 sq mm
Priority time: 4-Dec-79 18:39:39
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>TILOVEUR.CIF;1
File creation date: 4-Dec-79 18:39:39
Bounding box = 1934 x 1326 microns, Area = 2.56 sq mm

✔ WatanabeUR

Designer: Yuki Watanabe
Description: Sorter slice
Est.BB: 2300 x 2600 micron

Design is awaiting allocation.
Required space = 2008 x 2240 microns, Area = 4.50 sq mm
Priority time: 4-Dec-79 19:09:22
Current submittal is acceptable for implementation.
File name: [Maxc]<UOFR-VLSI>WATANABEUR.CIF;2
File creation date: 4-Dec-79 19:09:22
Bounding box = 2008 x 2240 microns, Area = 4.50 sq mm

UofR

Summary of designs from UofR, updated 4-Dec-79 3:51:33

ErmerUR

Implementer: Rick Ermer and Tuan Nguyen
Description: Speedometer/Odometer
Est.BB: 2000 microns x 3750 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

KahrsUR

Designer: Mark Kahrs
Description: 13 bit DAC
Est.BB: 2500 x 1500 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

KedemUR

Designers(s): Gershon Kedem and Michel Denber
Description: Infinite precision multiplier
Est.BB: ~ 2000 x 2000 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

LylesUR

Implementer: Brian Lyles
Description: Interpolative A/D
Est.BB: 2000 microns x 1250 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

LyonsUR

Implementer: Bob Lyons
Description: Programmable Frequency Generator
Est.BB: 3000 microns x 3000 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

RajUR

Implementer: Raj
Description: CAM
Est.BB: 2000 microns x 500 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

SabbahUR

Designer: Danny Sabbah
Description: Programmable SLA
Est.BB: ~ 4600 x 5500 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

SohmUR

Designers: Larry Sohm, Pat Chan, Bill Notowitz

Description: Digital Phase lock loop
Est.BB: 1500 x 3000 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

TiloveUR

Designer(s): Bob Tilove, Jarek Rossignac
Description: This is a bit slice coordinate transformer
Est. BB: ~ 1400 X 2000 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

UofR Priority:

- Watanabe
- Kelley — on [Marc] <Lyon>
- Lyons
- Sohns

- TiloverUR.CIF — on [Marc] <Lyon>

Sabbah — Some calculations. Figuratively wasteful of space

Kahrs	N.G.
Lyles	N.G.
Raj	N.G.

Memo from: LYNN CONWAY

SU SUMMARY:

19 proj.	79.16 mm²

+ HIT LIST:

5 proj. 28.66 mm²

3

XEROX

SU FINAL

Summary of designs from SU, updated 4-Dec-79 20:40:30

✓ AtlasSU

Designer(s): Les Atlas, Doug Galbraith
Description: This project is an neural-stim. interval timer
Est.BB: ~ 2500 x 2000 microns. *

Space is allocated.
Reserved space = 2478 x 1378 microns, Area = 3.41 sq mm
Priority time: 30-Nov-79 23:42:48
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ATLASSU.CIF;4
File creation date: 4-Dec-79 16:28:09
Bounding box = 2478 x 1378 microns, Area = 3.41 sq mm

✓ BasкettSU

Designer(s): Forest Baskett
Description: This project is an Ethernet synchronizer
Est.BB: ~ 2250 X 2500 microns.

Space is allocated.
Reserved space = 2240 x 2720 microns, Area = 6.09 sq mm
Priority time: 26-Nov-79 8:52:03
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>BASKETTSU.CIF;1
File creation date: 26-Nov-79 8:52:03
Bounding box = 2240 x 2720 microns, Area = 6.09 sq mm

✓ BectolsheimSU

Designer(s): Andy Bechtolsheim, Thomas Gross
Description: This project is a parallel search table for log arithmetic
Est.BB: ~ 3500 X 1800 microns.

Space is allocated.
Reserved space = 1514 x 3180 microns, Area = 4.81 sq mm
Priority time: 23-Nov-79 15:41:04
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>BECTOLSHEIMSU.CIF;3
File creation date: 3-Dec-79 22:52:06
Bounding box = 1514 x 3180 microns, Area = 4.81 sq mm

✓ Clark2SU

Designer(s): Jim Clark
Description: This project is a self-timed clock element
Est BB: ~ 1200 x 1200 microns.

Design is awaiting allocation.
Required space = 1606 x 1688 microns, Area = 2.71 sq mm
Priority time: 1-Dec-79 19:02:59
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>CLARK2SU.CIF;3
File creation date: 4-Dec-79 13:21:54
Bounding box = 1606 x 1688 microns, Area = 2.71 sq mm

✓ ClarkSU

Designer(s): Jim Clark
Description: This project is a simple graphics ALU
Est.BB: ~ 3000 x 3000 microns

Space is allocated.
Reserved space = 2976 x 2764 microns, Area = 8.23 sq mm
Priority time: 28-Nov-79 14:57:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>CLARKSU.CIF;3
File creation date: 4-Dec-79 16:18:37
Bounding box = 2976 x 2764 microns, Area = 8.23 sq mm

ElahianSU

Designer(s): Kamran Elahian, Fred Basham
Description: This project is a UART line speed determiner
Est.BB: ~ 1950 X 1900 microns.

Space is allocated.
Reserved space = 1856 x 1856 microns, Area = 3.44 sq mm
Priority time: 1-Dec-79 16:11:10
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ELAHIANSU.CIF;3
File creation date: 4-Dec-79 15:34:00
Bounding box = 1856 x 1856 microns, Area = 3.44 sq mm

FrolikSU

Designer(s): Bill Frolik, Roderick Young
Description: This project is a digital timer
Est.BB: ~ 2750 x 2125 microns. *

Design is awaiting allocation.
Required space = 2120 x 2684 microns, Area = 5.69 sq mm
Priority time: 4-Dec-79 12:08:07
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>FROLIKSU.CIF;5
File creation date: 4-Dec-79 12:08:07
Bounding box = 2120 x 2684 microns, Area = 5.69 sq mm

GehlbachSU

Designer(s): Steve Gehlbach, Joe Sharp, Bill Jansen
Description: This project is a fast 16-input adder
Est.BB: ~ 1250 X 3250 microns. *

Space is allocated.
Reserved space = 3180 x 1856 microns, Area = 5.90 sq mm
Priority time: 30-Nov-79 8:36:06
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>GEHLBACHSU.CIF;6
File creation date: 4-Dec-79 11:49:07
Bounding box = 3180 x 1856 microns, Area = 5.90 sq mm

HannahSU

Designer(s): Peter Eichenberger, Marc Hannah
Description: This project is a rectangle generator
Est.BB: ~ 2000 X 2500 microns.

Space is allocated.
Reserved space = 2386 x 2140 microns, Area = 5.11 sq mm
Priority time: 30-Nov-79 21:33:31
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HANNAHSU.CIF;6
File creation date: 4-Dec-79 12:09:11
Bounding box = 2386 x 2140 microns, Area = 5.11 sq mm

HerndonSU

Designer(s): Matt Herndon, Jeff Thorson
Description: This project is a typesetting machine
Est.BB: ~ 2500 X 2250 microns.

Space is allocated.
Reserved space = 3170 x 2000 microns, Area = 6.34 sq mm
Priority time: 30-Nov-79 23:45:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HERNDONSU.CIF;2
File creation date: 3-Dec-79 22:42:50
Bounding box = 3170 x 2000 microns, Area = 6.34 sq mm

✔ MacomberSU

Designer(s): Scott Macomber, Bob Clark
Description: This project is a parallel/serial multiplier
Est.BB: ~ 1900 X 1900 microns.

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm
Priority time: 2-Dec-79 22:18:27
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MACOMBERSU.CIF;4
File creation date: 4-Dec-79 11:50:29
Bounding box = 2000 x 2000 microns, Area = 4.00 sq mm

✔ MarkeeSU

Designer(s): Pat Markee, Irene Watson
Description: This project is a digital clock
Est.BB: ~ 2000 X 3000 microns.

Space is allocated.
Reserved space = 2120 x 1424 microns, Area = 3.02 sq mm
Priority time: 30-Nov-79 21:52:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MARKEESU.CIF;2
File creation date: 4-Dec-79 15:38:53
Bounding box = 2120 x 1424 microns, Area = 3.02 sq mm

✔ MathewsSU

Designer(s): Rob Mathews, John Newkirk
Desciption: This project is the infamous Buffalo chip
Est.BB: ~ 5000 X 1250 microns.

Space is allocated.
Reserved space = 5180 x 1134 microns, Area = 5.87 sq mm
Priority time: 23-Nov-79 15:33:45
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MATHEWSSU.CIF;1
File creation date: 23-Nov-79 15:33:45
Bounding box = 5180 x 1134 microns, Area = 5.87 sq mm

✔ NoiceSU

Designer(s): David Noice, Neil Midkiff
Description: This project is a multiplier/divider
Est.BB: ~ 2750 X 1500 microns.

Space is allocated.
Reserved space = 2888 x 1576 microns, Area = 4.55 sq mm
Priority time: 1-Dec-79 16:14:51
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>NOICESU.CIF;2
File creation date: 4-Dec-79 15:20:56
Bounding box = 2888 x 1576 microns, Area = 4.55 sq mm

✔ OhChinSU

Designer(s): Soo-Young Oh, Dae-Je Chin
Description: This project is a automatic thermostat time controler
Est.BB: ~ 2150 X 1600 microns.

Space is allocated.
Reserved space = 2120 x 1700 microns, Area = 3.60 sq mm
Priority time: 30-Nov-79 8:33:40
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>OHCHINSU.CIF;3
File creation date: 4-Dec-79 9:02:42
Bounding box = 2120 x 1700 microns, Area = 3.60 sq mm

OyeSU HIT

Designer(s): Kevin Oye, Alan Siegel
Description: This project is a error-correcting parallel/serial interface
Est.BB: ~ 3000 X 2500 microns.

Design is awaiting allocation.
Required space = 1882 x 1486 microns, Area = 2.80 sq mm
Priority time: 4-Dec-79 17:00:38
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>OYESU.CIF;2
File creation date: 4-Dec-79 17:00:38
Bounding box = 1882 x 1486 microns, Area = 2.80 sq mm

StrongSU HIT

Designer(s): Alex Strong, Danny Sleator
Description: This project is a guitar chip
Est.BB: ~ 3000 X 1875 microns.

Design is awaiting allocation.
Required space = 1856 x 2120 microns, Area = 3.93 sq mm
Priority time: 4-Dec-79 17:03:35
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>STRONGSU.CIF;4
File creation date: 4-Dec-79 17:03:35
Bounding box = 1856 x 2120 microns, Area = 3.93 sq mm

SytwuSU HIT

Designer(s): J. Sytwu, Hamid Najafi
Description: This project is a quad PCM bus interface
Est.BB: ~ 3000 X 3000 microns.

Space is allocated.
Reserved space = 4150 x 3146 microns, Area = 13.06 sq mm
Priority time: 1-Dec-79 12:36:07
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>SYTWUSU.CIF;2
File creation date: 4-Dec-79 16:55:21
Bounding box = 4150 x 3146 microns, Area = 13.06 sq mm

✓ TarsiSU HIT

Designer(s): Mike Tarsi, Nagatsugu Yamanouchi
Description: This project is a multifunction digital clock
Est.BB: ~ 1920 X 1920 microns.

Design is awaiting allocation.
Required space = 2140 x 2276 microns, Area = 4.87 sq mm
Priority time: 1-Dec-79 12:56:09
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>TARSISU.CIF;3
File creation date: 4-Dec-79 12:10:50
Bounding box = 2140 x 2276 microns, Area = 4.87 sq mm

✓ UttSU HIT

Designer(s): Steve Utt, Shalom Ackelsberg
Description: This project is part of a pancreas prosthesis
Est B.B.: 2000 X 2000 microns

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm
Priority time: 1-Dec-79 12:56:46
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>UTTSU.CIF;3
File creation date: 4-Dec-79 11:55:45
Bounding box = 2000 x 2000 microns, Area = 4.00 sq mm

✓ WulffSU

Designer(s): Bob Wulff, Tom Bennett
Description: This project is a bit slice of a multiplier
Est.BB: ~ 2375 X 2125 microns.

Design is awaiting allocation.
Required space = 2120 x 1856 microns, Area = 3.93 sq mm
Priority time: 3-Dec-79 20:31:30
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>WULFFSU.CIF;3
File creation date: 4-Dec-79 12:12:38
Bounding box = 2120 x 1856 microns, Area = 3.93 sq mm

✓ ZarghanSU

Designer(s): Bahman Zargham, Jerry Huck
Description: This project is a multiplexed communications link
Est.BB: ~ 2250 X 1900 microns.

Space is allocated.
Reserved space = 1590 x 1550 microns, Area = 2.46 sq mm
Priority time: 30-Nov-79 21:36:20
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ZARGHANSU.CIF;4
File creation date: 3-Dec-79 23:03:11
Bounding box = 1590 x 1550 microns, Area = 2.46 sq mm

SU

Summary of designs from SU, updated 4-Dec-79 3:51:33

AhmedSU

Designer(s): Hassan Ahmed, Rich Baker
Description: This project is a forward error-correction codec
Est.BB: ~ 1250 X 2250 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

AtlasSU

Designer(s): Les Atlas, Doug Galbraith
Description: This project is an neural-stim. interval timer
Est.BB: ~ 2500 x 2000 microns. *

Space is allocated.
Reserved space = 2478 x 1378 microns, Area = 3.41 sq mm
Priority time: 30-Nov-79 23:42:48
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ATLASSU.CIF;3
File creation date: 3-Dec-79 22:37:44
Bounding box = 2478 x 1378 microns, Area = 3.41 sq mm

BaskettSU

Designer(s): Forest Baskett
Description: This project is an Ethernet synchronizer
Est.BB: ~ 2250 X 2500 microns.

Space is allocated.
Reserved space = 2240 x 2720 microns, Area = 6.09 sq mm
Priority time: 26-Nov-79 8:52:03
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>BASKETTSU.CIF;1
File creation date: 26-Nov-79 8:52:03
Bounding box = 2240 x 2720 microns, Area = 6.09 sq mm

BectolsheimSU

Designer(s): Andy Bechtolsheim, Thomas Gross
Description: This project is a parallel search table for log arithmetic
Est.BB: ~ 3500 X 1800 microns.

Space is allocated.
Reserved space = 1514 x 3180 microns, Area = 4.81 sq mm
Priority time: 23-Nov-79 15:41:04
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>BECTOLSHEIMSU.CIF;3
File creation date: 3-Dec-79 22:52:06
Bounding box = 1514 x 3180 microns, Area = 4.81 sq mm

Clark2SU

Designer(s): Jim Clark
Description: This project is a self-timed clock element
Est BB: ~ 1200 x 1200 microns.

Space is allocated.
Reserved space = 1630 x 1642 microns, Area = 2.68 sq mm
Priority time: 1-Dec-79 19:02:59
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>CLARK2SU.CIF;2
File creation date: 3-Dec-79 0:09:46
Bounding box = 1630 x 1642 microns, Area = 2.68 sq mm

ClarkSU

Designer(s): Jim Clark

Description: This project is a simple graphics ALU
Est.BB: ~ 3000 x 3000 microns

Space is allocated.
Reserved space = 2764 x 2976 microns, Area = 8.23 sq mm
Priority time: 28-Nov-79 14:57:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>CLARKSU.CIF;1
File creation date: 28-Nov-79 14:57:42
Bounding box = 2764 x 2976 microns, Area = 8.23 sq mm

ElahianSU

Designer(s): Kamran Elahian, Fred Basham
Description: This project is a UART line speed determiner
Est.BB: ~ 1950 X 1900 microns.

Space is allocated.
Reserved space = 1856 x 1856 microns, Area = 3.44 sq mm
Priority time: 1-Dec-79 16:11:10
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ELAHIANSU.CIF;2
File creation date: 3-Dec-79 22:59:42
Bounding box = 1856 x 1856 microns, Area = 3.44 sq mm

ErbilSU

Designer(s): Oktay Erbil, Peter Fu
Description: This project is a consistency unit for a fault-tolerant system
Est.BB: ~ 2250 X 1950 microns.

Space is allocated.
Reserved space = 2250 x 2500 microns, Area = 5.63 sq mm
Priority time: 2-Dec-79 22:17:37
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ERBILSU.CIF;2
File creation date: 2-Dec-79 22:17:37
Bounding box = 2250 x 2500 microns, Area = 5.63 sq mm

FrolikSU

Designer(s): Bill Frolik, Roderick Young
Description: This project is a digital timer
Est.BB: ~ 2750 x 2125 microns. *

Design is not ready for space allocation.
Current submittal is not implementable.
File name: [Maxc]<SU-VLSI>FROLIKSU.CIF;4
File creation date: 1-Dec-79 15:49:41

GehlbachSU

Designer(s): Steve Gehlbach, Joe Sharp, Bill Jansen
Description: This project is a fast 16-input adder
Est.BB: ~ 1250 X 3250 microns. *

Space is allocated.
Reserved space = 3180 x 1856 microns, Area = 5.90 sq mm
Priority time: 30-Nov-79 8:36:06
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>GEHLBACHSU.CIF;5
File creation date: 3-Dec-79 9:30:45
Bounding box = 3180 x 1856 microns, Area = 5.90 sq mm

GlussSU

Designer(s): Dave Gluss, Bill Nowicki
Description: This project is a Ethernet deserializing buffer
Est.BB: ~ 5000 X 1250 microns.

Space is allocated.

Reserved space = 3180 x 1644 microns, Area = 5.23 sq mm
Priority time: 1-Dec-79 12:31:33
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>GLUSSSU.CIF;1
File creation date: 1-Dec-79 12:31:33
Bounding box = 3180 x 1644 microns, Area = 5.23 sq mm

HannahSU

Designer(s): Peter Eichenberger, Marc Hannah
Description: This project is a rectangle generator
Est.BB: ~ 2000 X 2500 microns.

Space is allocated.
Reserved space = 2386 x 2140 microns, Area = 5.11 sq mm
Priority time: 30-Nov-79 21:33:31
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HANNAHSU.CIF;6
File creation date: 3-Dec-79 16:43:58
Bounding box = 2386 x 2140 microns, Area = 5.11 sq mm

HerndonSU

Designer(s): Matt Herndon, Jeff Thorson
Description: This project is a typesetting machine
Est.BB: ~ 2500 X 2250 microns.

Space is allocated.
Reserved space = 3170 x 2000 microns, Area = 6.34 sq mm
Priority time: 30-Nov-79 23:45:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HERNDONSU.CIF;2
File creation date: 3-Dec-79 22:42:50
Bounding box = 3170 x 2000 microns, Area = 6.34 sq mm

HorowitzSU

Designer(s): Mark Horowitz, Wayne Wolf
Description: This project is a model train speed controller
Est.BB: ~ 2000 X 2125 microns.

Design is awaiting allocation.
Required space = 2430 x 2160 microns, Area = 5.25 sq mm
Priority time: 3-Dec-79 20:29:55
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HOROWITZSU.CIF;2
File creation date: 3-Dec-79 20:29:55
Bounding box = 2430 x 2160 microns, Area = 5.25 sq mm

HuangSU

Designer(s): Wen-her Huang
Description: This project is a CAM
Est.BB: ~ 2000 X 2000 microns.

Design is awaiting allocation.
Required space = 2100 x 2000 microns, Area = 4.20 sq mm
Priority time: 3-Dec-79 16:45:54
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HUANGSU.CIF;1
File creation date: 3-Dec-79 16:45:54
Bounding box = 2100 x 2000 microns, Area = 4.20 sq mm

KarmarkarSU

Designer(s): Narendra Karmarkar, Timothy Gonsalves
Description: This project is a bit-slice residue autocorrelator
Est.BB: ~ 2000 X 2125 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

MacomberSU

Designer(s): Scott Macomber, Bob Clark
Description: This project is a parallel/serial multiplier
Est.BB: ~ 1900 X 1900 microns.

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm
Priority time: 2-Dec-79 22:18:27
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MACOMBERSU.CIF;3
File creation date: 2-Dec-79 22:18:27
Bounding box = 2000 x 2000 microns, Area = 4.00 sq mm

MarkeeSU

Designer(s): Pat Markee, Irene Watson
Description: This project is a digital clock
Est.BB: ~ 2000 X 3000 microns.

Space is allocated.
Reserved space = 2120 x 1424 microns, Area = 3.02 sq mm
Priority time: 30-Nov-79 21:52:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MARKEESU.CIF;1
File creation date: 30-Nov-79 21:52:42
Bounding box = 2120 x 1424 microns, Area = 3.02 sq mm

MathewsSU

Designer(s): Rob Mathews, John Newkirk
Desciption: This project is the infamous Buffalo chip
Est.BB: ~ 5000 X 1250 microns.

Space is allocated.
Reserved space = 5180 x 1134 microns, Area = 5.87 sq mm
Priority time: 23-Nov-79 15:33:45
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MATHEWSSU.CIF;1
File creation date: 23-Nov-79 15:33:45
Bounding box = 5180 x 1134 microns, Area = 5.87 sq mm

NoiceSU

Designer(s): David Noice, Neil Midkiff
Description: This project is a multiplier/divider
Est.BB: ~ 2750 X 1500 microns.

Space is allocated.
Reserved space = 2888 x 1576 microns, Area = 4.55 sq mm
Priority time: 1-Dec-79 16:14:51
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>NOICESU.CIF;1
File creation date: 1-Dec-79 16:14:51
Bounding box = 2888 x 1576 microns, Area = 4.55 sq mm

OhChinSU

Designer(s): Soo-Young Oh, Dae-Je Chin
Description: This project is a automatic thermostat time controler
Est.BB: ~ 2150 X 1600 microns.

Space is allocated.
Reserved space = 2120 x 1700 microns, Area = 3.60 sq mm
Priority time: 30-Nov-79 8:33:40
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>OHCHINSU.CIF;2
File creation date: 30-Nov-79 8:33:40
Bounding box = 2120 x 1700 microns, Area = 3.60 sq mm

OyeSU

Designer(s): Kevin Oye, Alan Siegel
Description: This project is a error-correcting parallel/serial interface
Est.BB: ~ 3000 X 2500 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

RedfordSU

Designer(s): John Redford, Lyle Smith
Description: This project is a self test memory
Est.BB: ~ 3125 x 2875 microns

Space is allocated.
Reserved space = 2126 x 2776 microns, Area = 5.90 sq mm
Priority time: 1-Dec-79 12:33:37
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>REDFORDSU.CIF;1
File creation date: 1-Dec-79 12:33:37
Bounding box = 2126 x 2776 microns, Area = 5.90 sq mm

StrongSU

Designer(s): Alex Strong, Danny Sleator
Description: This project is a guitar chip
Est.BB: ~ 3000 X 1875 microns.

Design is not ready for space allocation.
Current submittal is not implementable.
File name: [Maxc]<SU-VLSI>STRONGSU.CIF;2
File creation date: 1-Dec-79 15:45:03

SytwuSU

Designer(s): J. Sytwu, Hamid Najafi
Description: This project is a quad PCM bus interface
Est.BB: ~ 3000 X 3000 microns.

Space is allocated.
Reserved space = 3000 x 2546 microns, Area = 7.64 sq mm
Priority time: 1-Dec-79 12:36:07
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>SYTWUSU.CIF;1
File creation date: 1-Dec-79 12:36:07
Bounding box = 3000 x 2546 microns, Area = 7.64 sq mm

TarsiSU

Designer(s): Mike Tarsi, Nagatsugu Yamanouchi
Description: This project is a multifunction digital clock
Est.BB: ~ 1920 X 1920 microns.

Design is awaiting allocation.
Required space = 2140 x 2276 microns, Area = 4.87 sq mm
Priority time: 1-Dec-79 12:56:09
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>TARSISU.CIF;2
File creation date: 3-Dec-79 16:46:34
Bounding box = 2140 x 2276 microns, Area = 4.87 sq mm

UttSU

Designer(s): Steve Utt, Shalom Ackelsberg
Description: This project is part of a pancreas prosthesis
Est B.B.: 2000 X 2000 microns

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm

Priority time: 1-Dec-79 12:56:46
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>UTTSU.CIF;2
File creation date: 1-Dec-79 12:56:46
Bounding box = 2000 x 2000 microns, Area = 4.00 sq mm

WulffSU

Designer(s): Bob Wulff, Tom Bennett
Description: This project is a bit slice of a multiplier
Est.BB: ~ 2375 X 2125 microns.

Design is awaiting allocation.
Required space = 2120 x 1856 microns, Area = 3.93 sq mm
Priority time: 3-Dec-79 20:31:30
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>WULFFSU.CIF;2
File creation date: 3-Dec-79 20:31:30
Bounding box = 2120 x 1856 microns, Area = 3.93 sq mm

ZarghanSU

Designer(s): Bahman Zargham, Jerry Huck
Description: This project is a multiplexed communications link
Est.BB: ~ 2250 X 1900 microns.

Space is allocated.
Reserved space = 1590 x 1550 microns, Area = 2.46 sq mm
Priority time: 30-Nov-79 21:36:20
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ZARGHANSU.CIF;4
File creation date: 3-Dec-79 23:03:11
Bounding box = 1590 x 1550 microns, Area = 2.46 sq mm

SU Priorities

(1) M. Trews, Baskett, Bechtolsheim, Clark

(2) Atlas, Herndon, Noire, OhChin, Frolik, Hannah, Gehlbach, Macomber, Elahian, Wulff, Zarghan

(3) Markee, Utt, Tarpi

(4) Sytwu

(5) Oye, Strong

(494-2959)

HIT

MPC79 Wafer Partitioning:

Memo from: LYNN CONWAY

WAFER PARTITIONING:

SUGGESTION:

A		B	
MIT	91.23	CALTECH	94.28
OTH	65.50	SU	79.16
ILL	38.91	U of R	30.34
CMU	28.10	UCB	21.81
	223.74		225.59

XEROX

WAFER A			WAFER B		
B	MIT2		I	SU2	
C	MIT1	Glasser	J	CT1	
D	ILL		K	SU1	
E	CMU	UIclass Mavrik Rogers	L	CT 2	
F	SCMP		M	UCB	(+CT)
G	MIT3	Snyder Wolf CT	N	UR	(+SU)
H	DOC		O	DOC	

ESTIMATE OF AVAILABLE AREA:

$$A = (12 \text{ die}) \times (5.926\,mm) \times (7.548\,mm) \times D_p$$
$$= 12 \times 44.73\,mm^2 \times D_p$$
$$= 536.75\,D_p$$

Now D_p: $\quad \sim .75 < D_p < \sim .93$

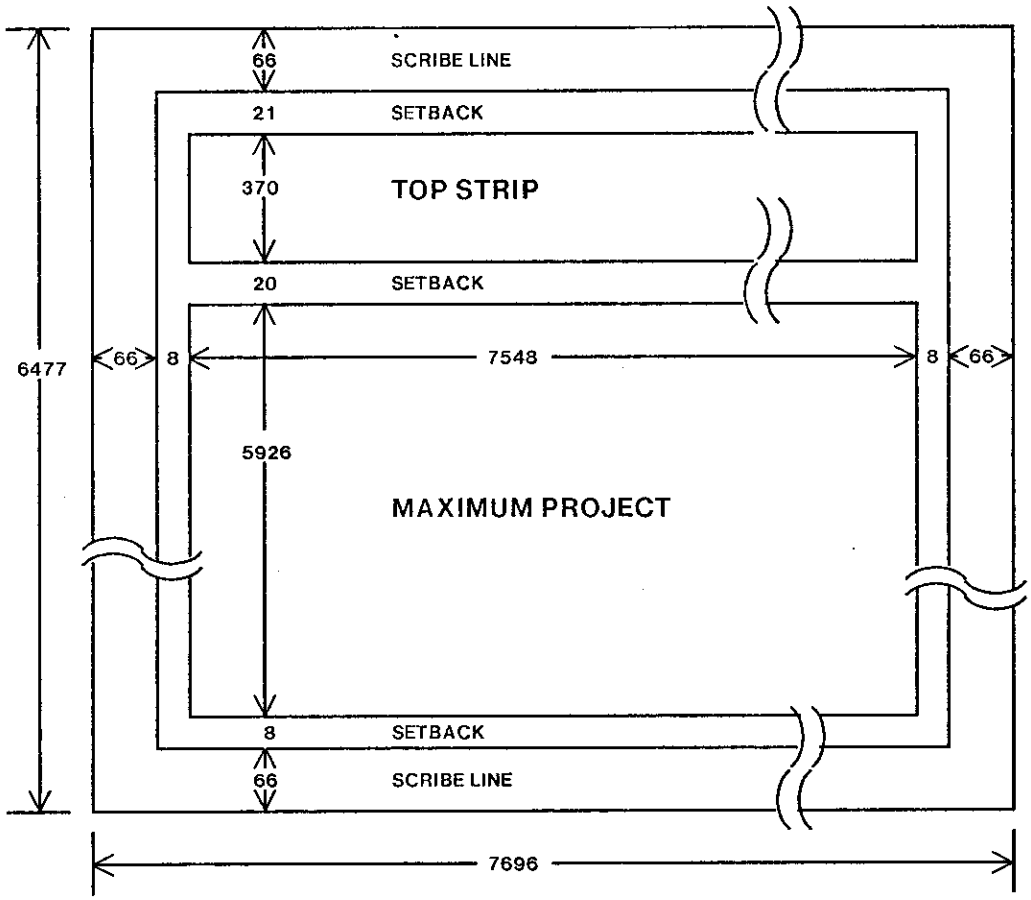
$$\therefore \quad 400\,mm^2 < A < 500\,mm^2$$

DEMAND

	PR.	MM^2	HIT LIST PR.	HIT LIST MM^2
MIT	15	91.23		
CALTECH	22	94.28	2	9.83
STANFORD	17	79.16	5	28.66
UCB	4	21.81		
ILLINOIS	5	38.91		
CMU	5	28.10		
U of R	5	30.34		
OTHER	6	65.50		
	79	449.33	7	38.49

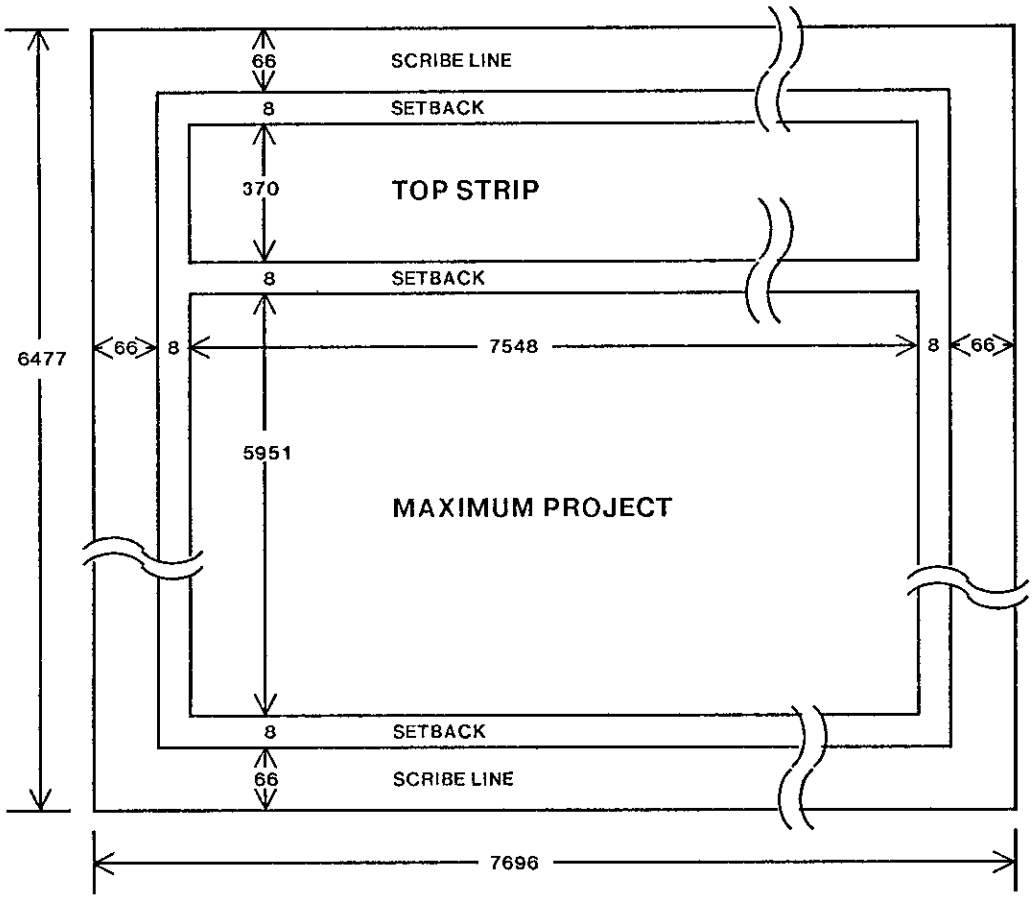
WILL FILL IF $D_p \cong .84$

MPC79 Scribe Lines:

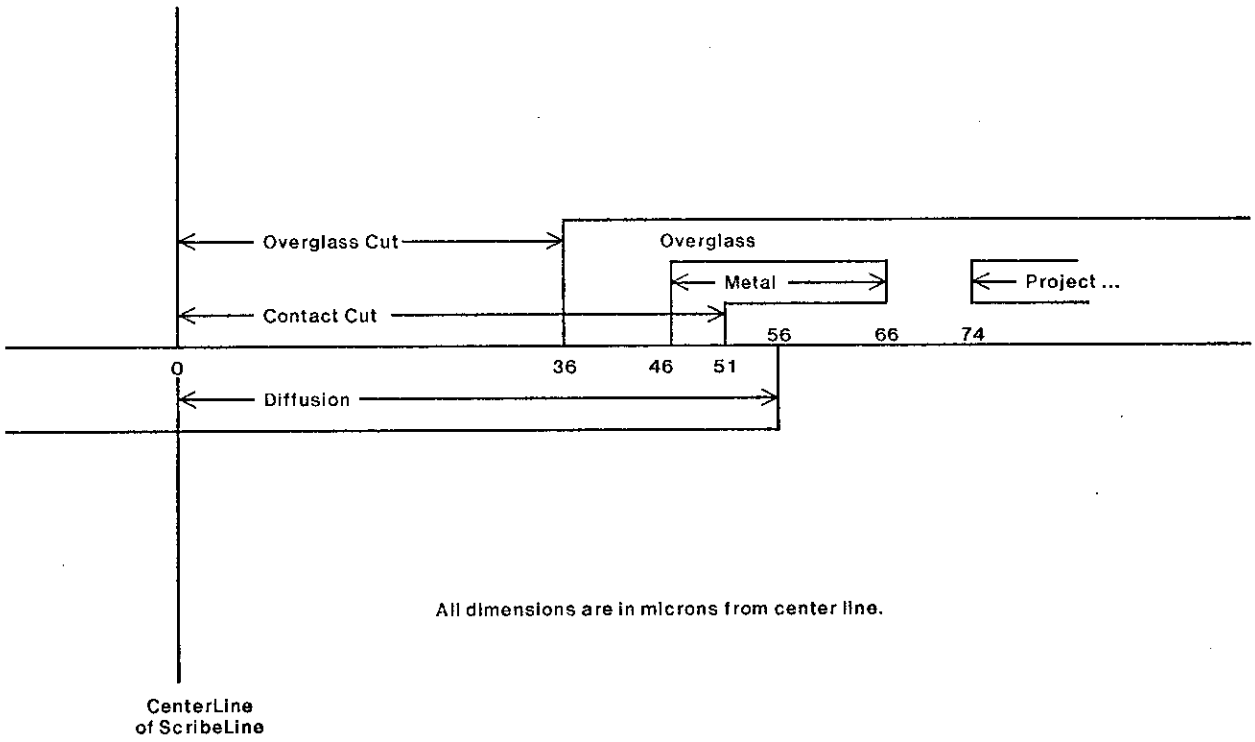


Dimensions are in Microns
Not drawn to Scale

XEROX PARC	Project MPC79	Title Chip Layout	File ChipLayout.Sil	Designer Pasco	Rev B	Date 12/3/79	Page 01



XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	MPC79	Chip Layout	ChipLayout.Sil	Pasco	A	12/1/79	01



XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	MPC79	Scribe Line Profile	ScribeLine.Sil	Pasco	A	11/25/79	01

MPC79 Final Merge Specification:

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:55:32;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: A =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: H =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79AH.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: RHDoc1 =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3583 735;
   File: [Ivy]<Mpc79>RHDoc1.cif;

  PROJECT: LhDoc1 =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 48 793;
   File: [Ivy]<Mpc79>LhDoc1.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:56:03;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: A =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: C =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79AC.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: GlasserOT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 655 991;
   File: [Ivy]<Mpc79>GlasserOT.cif;

  PROJECT: PasemanMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3377 2877;
   File: [Ivy]<Mpc79>PasemanMIT.cif;

  PROJECT: ChuMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 4435 1183;
   File: [Ivy]<Mpc79>ChuMIT.cif;

  PROJECT: HamiltonMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
  Rotation: 1 0;
  Translation: 265 3163;
  File: [Ivy]<Mpc79>HamiltonMIT.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:56:46;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: A =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: B =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79AB.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: KhouryMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 130 2381;
   File: [Ivy]<Mpc79>KhouryMIT.cif;

  PROJECT: GrondalskiMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 128 114;
   File: [Ivy]<Mpc79>GrondalskiMIT.cif;

  PROJECT: GoodrichMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 2736 2246;
   File: [Ivy]<Mpc79>GoodrichMIT.cif;

  PROJECT: PicardMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 2762 188;
   File: [Ivy]<Mpc79>PicardMIT.cif;

  PROJECT: BataliMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 130 4167;
   File: [Ivy]<Mpc79>BataliMIT.cif;

  PROJECT: AllenMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5257 2651;
   File: [Ivy]<Mpc79>AllenMIT.cif;

  PROJECT: FichtenbaumMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 4962 3408;
   File: [Ivy]<Mpc79>FichtenbaumMIT.cif;

  PROJECT: GramlichMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 4597 3999;
   File: [Ivy]<Mpc79>GramlichMIT.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:55:39;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: A =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: G =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79AG.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: SynderOT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 275 569;
   File: [Ivy]<Mpc79>SynderOT.cif;

  PROJECT: RivestMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 7393 3645;
   File: [Ivy]<Mpc79>RivestMIT.cif;

  PROJECT: KathailMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 4413 4187;
   File: [Ivy]<Mpc79>KathailMIT.cif;

  PROJECT: GoddeauMIT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 4471 241;
   File: [Ivy]<Mpc79>GoddeauMIT.cif;

  PROJECT: WalpCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 263 3829;
   File: [Ivy]<Mpc79>WalpCT.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:55:46;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: A =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: F =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79AF.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: Schip2 =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 74 74;
   File: [Ivy]<Mpc79>Schip2.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:57:26;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: A =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: D =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79AD.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: HanesUI =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 4758 3148;
   File: [Ivy]<Mpc79>HanesUI.cif;

  PROJECT: AdrianUI =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 4585 261;
   File: [Ivy]<Mpc79>AdrianUI.cif;

  PROJECT: LuhukayUI =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 4072 3218;
   File: [Ivy]<Mpc79>LuhukayUI.cif;

  PROJECT: MontoyeUI =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
  Rotation: 1 0;
  Translation: 4777 253;
  File: [Ivy]<Mpc79>MontoyeUI.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:55:53;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: A =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: E =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79AE.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: MurrayOT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3206 4826;
   File: [Ivy]<Mpc79>MurrayOT.cif;

  PROJECT: RodgersOT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 1955 1005;
   File: [Ivy]<Mpc79>RodgersOT.cif;

  PROJECT: ClassUI =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 1141 4427;
   File: [Ivy]<Mpc79>ClassUI.cif;

  PROJECT: KungCMU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 1182 118;
   File: [Ivy]<Mpc79>KungCMU.cif;

  PROJECT: KehlOT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 6169 1078;
   File: [Ivy]<Mpc79>KehlOT.cif;

  PROJECT: HoeyCMU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 4288 114;
   File: [Ivy]<Mpc79>HoeyCMU.cif;

  PROJECT: EbelingCMU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 6660 5050;
   File: [Ivy]<Mpc79>EbelingCMU.cif;

  PROJECT: GuptaCMU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 696 352;
   File: [Ivy]<Mpc79>GuptaCMU.cif;

  PROJECT: SongCMU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 4764 2141;
   File: [Ivy]<Mpc79>SongCMU.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:56:18;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: B =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: O =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79BO.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: RHDoc2 =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3602 695;
   File: [Ivy]<Mpc79>RHDoc2.cif;

  PROJECT: LhDoc2 =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 53 757;
   File: [Ivy]<Mpc79>LhDoc2.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:55:10;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: B =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: J =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79BJ.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: CocconiCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 2583 2330;
   File: [Ivy]<Mpc79>CocconiCT.cif;

  PROJECT: CampbellCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 146 4296;
   File: [Ivy]<Mpc79>CampbellCT.cif;

  PROJECT: PursifullCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3153 2267;
   File: [Ivy]<Mpc79>PursifullCT.cif;

  PROJECT: FuCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 2089 4335;
   File: [Ivy]<Mpc79>FuCT.cif;

  PROJECT: TannerCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5562 74;
   File: [Ivy]<Mpc79>TannerCT.cif;

  PROJECT: WhitneyCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3534 109;
   File: [Ivy]<Mpc79>WhitneyCT.cif;

  PROJECT: BartonCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 123 2154;
   File: [Ivy]<Mpc79>BartonCT.cif;

  PROJECT: BozzutoCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5373 4477;
   File: [Ivy]<Mpc79>BozzutoCT.cif;

  PROJECT: KingsleyCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 142 74;
   File: [Ivy]<Mpc79>KingsleyCT.cif;

  PROJECT: HoCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
```

```
   Translation: 3477 112;
   File: [Ivy]<Mpc79>HoCT.cif;

  PROJECT: LiCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5362 4639;
   File: [Ivy]<Mpc79>LiCT.cif;

  PROJECT: PapachCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 5179 3938;
   File: [Ivy]<Mpc79>PapachCT.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:54:50;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: B =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: L =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79BL.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: MostellerCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 862 334;
   File: [Ivy]<Mpc79>MostellerCT.cif;

  PROJECT: HellerCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 873 5248;
   file: [Ivy]<Mpc79>HellerCT.cif;

  PROJECT: GrayCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3795 2996;
   File: [Ivy]<Mpc79>GrayCT.cif;

  PROJECT: WatteyneCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 7516 3900;
   File: [Ivy]<Mpc79>WatteyneCT.cif;

  PROJECT: DerbyCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 5283 1754;
   File: [Ivy]<Mpc79>DerbyCT.cif;

  PROJECT: PedersenCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5698 74;
   File: [Ivy]<Mpc79>PedersenCT.cif;

  PROJECT: EatonCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3142 4488;
   File: [Ivy]<Mpc79>EatonCT.cif;

  PROJECT: PinesCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5756 2090;
   File: [Ivy]<Mpc79>PinesCT.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:57:47;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: B =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: K =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79BK.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: Clark2SU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 1363 4088;
   File: [Ivy]<Mpc79>Clark2SU.cif;

  PROJECT: ClarkSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 4775 132;
   File: [Ivy]<Mpc79>ClarkSU.cif;

  PROJECT: BaskettSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5288 5892;
   File: [Ivy]<Mpc79>BaskettSU.cif;

  PROJECT: MathewsSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 1339 134;
   File: [Ivy]<Mpc79>MathewsSU.cif;

  PROJECT: ZarghanSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 2927 4297;
   File: [Ivy]<Mpc79>ZarghanSU.cif;

  PROJECT: FrolikSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3038 5872;
   File: [Ivy]<Mpc79>FrolikSU.cif;

  PROJECT: BectolsheimSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3719 2156;
   File: [Ivy]<Mpc79>BectolsheimSU.cif;

  PROJECT: OhChinSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 3072 168;
   File: [Ivy]<Mpc79>OhChinSU.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:55:18;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: B =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: I =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79BI.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: AtlasSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5071 2583;
   File: [Ivy]<Mpc79>AtlasSU.cif;

  PROJECT: HannahSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3297 102;
   File: [Ivy]<Mpc79>HannahSU.cif;

  PROJECT: NoiceSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 83 2232;
   File: [Ivy]<Mpc79>NoiceSU.cif;

  PROJECT: HerndonSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 74 130;
   File: [Ivy]<Mpc79>HerndonSU.cif;

  PROJECT: GehlbachSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 2200 4132;
   File: [Ivy]<Mpc79>GehlbachSU.cif;

  PROJECT: MarkeeSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5432 4268;
   File: [Ivy]<Mpc79>MarkeeSU.cif;

  PROJECT: MacomberSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 130 3896;
   File: [Ivy]<Mpc79>MacomberSU.cif;

  PROJECT: WulffSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 7574 84;
   File: [Ivy]<Mpc79>WulffSU.cif;

  PROJECT: ElahianSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3114 2260;
   File: [Ivy]<Mpc79>ElahianSU.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:54:20;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: B =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: M =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79BM.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: LandmanUCB =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 124 1743;
   File: [Ivy]<Mpc79>LandmanUCB.cif;

  PROJECT: RumphCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 3706 1665;
   File: [Ivy]<Mpc79>RumphCT.cif;

  PROJECT: EllisCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 7574 1208;
   File: [Ivy]<Mpc79>EllisCT.cif;

  PROJECT: LigockiCT =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 144 1848;
   File: [Ivy]<Mpc79>LigockiCT.cif;

  PROJECT: DecuirUCB =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 2297 2669;
   File: [Ivy]<Mpc79>DecuirUCB.cif;

  PROJECT: FungUCB =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5068 3291;
   File: [Ivy]<Mpc79>FungUCB.cif;

  PROJECT: SequinUCB =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 6324 640;
   File: [Ivy]<Mpc79>SequinUCB.cif;
END
```

```
Comment: MPC document generated from MPC data base
                5-Dec-79  2:53:42;

Title: MPC79
Date: 113079
Account: ?????

MASKSET: B =
 Resolution: 2;
 Size: 100000 100000;
 Layers:
  diffusion = 10 DI,
  implant = 20 IM,
  poly = 30 PO,
  cut = 40 CU,
  metal = 50 ME,
  glass = 60 PA;

 CHIP: N =
  Dimensions: 7696 6477;
  Positions: 0 0;

  PROJECT: MPC79BN.MPC =
   Layers:
    ND = diffusion 0,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0,
    SND diffusion 1.5;
   Rotation: 1 0;
   Translation: 0 0;
   File: [Ivy]<Mpc79>Frame>FrameBM.cif;

  PROJECT: WatanabeUR =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 126 5955;
   File: [Ivy]<Mpc79>WatanabeUR.cif;

  PROJECT: LyonsUR =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 2160 5975;
   File: [Ivy]<Mpc79>LyonsUR.cif;

  PROJECT: UttSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 3094 111;
   File: [Ivy]<Mpc79>UttSU.cif;

  PROJECT: SohmUR =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
```

```
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 0 1;
   Translation: 137 74;
   File: [Ivy]<Mpc79>SohmUR.cif;

  PROJECT: KedemUR =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 4924 5980;
   File: [Ivy]<Mpc79>KedemUR.cif;

  PROJECT: TiloveUR =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 2842 3597;
   File: [Ivy]<Mpc79>TiloveUR.cif;

  PROJECT: TarsiSU =
   Layers:
    ND = diffusion 1.5,
    NI = implant 0,
    NP = poly 0,
    NC = cut 0,
    NM = metal 0,
    NG = glass 0;
   Rotation: 1 0;
   Translation: 5382 127;
   File: [Ivy]<Mpc79>TarsiSU.cif;
END
```

MPC79 MEBES Master Plate Specs:

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, CA 94304
December 3, 1979
5

To: Micro Mask, Inc.

From: Alan Bell (494-4326), Reference: P.O. #40784

Subject: MEBES Master Plate Specifications for project: **MPC79A**

Max. Pattern Dimensions : X: 7696 μm Y: 6477 μm
Step and Repeat distances: X: 7696 μm Y: 6477 μm

# Plates per Set:	6	Defect Density:	Standard
Plate Material:	Chrome, L.E. 30	Tolerance:	+/- 0.25 μm
Plate Size:	4" x 4" x 0.60"	CD width:	(see below)
E-beam Spot Size:	0.50 μm	Oversizing:	None
Pattern Size:	3", Round	Undersizing:	None

Pattern Specifications: There are seven (7) different project dies (named B, C, D, E, F, G, H) in this mask set. All have identical dimensions (7696 x 6477 microns). See the diagram on the following pages for the placements of die types within the mask set, and for the location of the CD's. For the purposes of this description, the six master plates will have the following plate names: DIF, IMP, POL, CUT, MET, PAD. The dies will be supplied on magtape in MEBES format.

Filenames for each layer are given in the following table (file names as a function of mask level/die type):

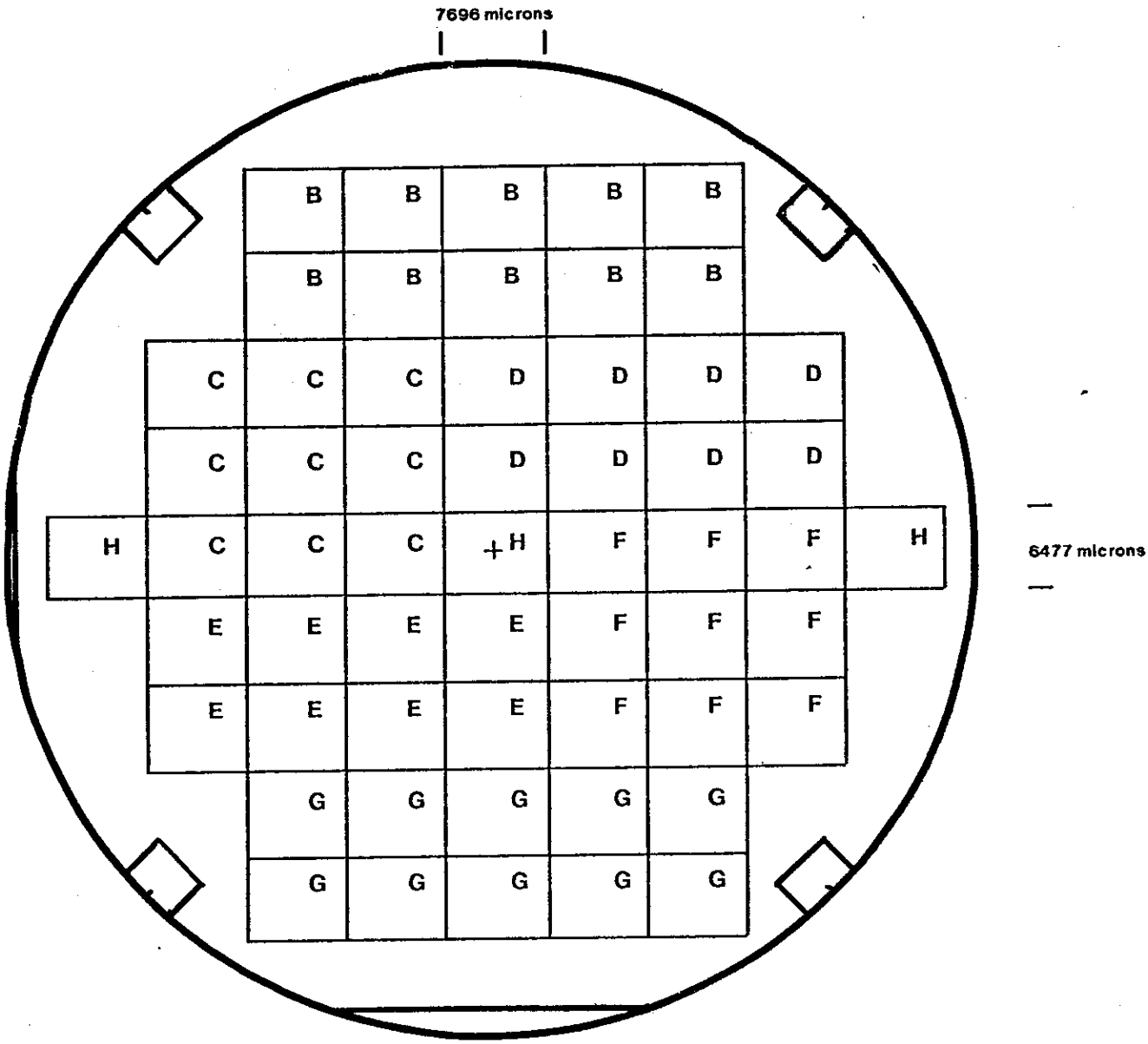
	DIF	IMP	POL	CUT	MET	PAD
Die B:	MPC79AB-10-DI	MPC79AB-20-IM	MPC79AB-30-PO	MPC79AB-40-CU	MPC79AB-50-ME	MPC79AB-60-PA
Die C:	MPC79AC-10-DI	MPC79AC-20-IM	MPC79AC-30-PO	MPC79AC-40-CU	MPC79AC-50-ME	MPC79AC-60-PA
Die D:	MPC79AD-10-DI	MPC79AD-20-IM	MPC79AD-30-PO	MPC79AD-40-CU	MPC79AD-50-ME	MPC79AD-60-PA
Die E:	MPC79AE-10-DI	MPC79AE-20-IM	MPC79AE-30-PO	MPC79AE-40-CU	MPC79AE-50-ME	MPC79AE-60-PA
Die F:	MPC79AF-10-DI	MPC79AF-20-IM	MPC79AF-30-PO	MPC79AF-40-CU	MPC79AF-50-ME	MPC79AF-60-PA
Die G:	MPC79AG-10-DI	MPC79AG-20-IM	MPC79AG-30-PO	MPC79AG-40-CU	MPC79AG-50-ME	MPC79AG-60-PA
Die H:	MPC79AH-10-DI	MPC79AH-20-IM	MPC79AH-30-PO	MPC79AH-40-CU	MPC79AH-50-ME	MPC79AH-60-PA

PLEASE adjust the patterns so that the TEXT on the mask is WRONG-READING when viewed from the CHROME SIDE.

DEVICE LABEL (to appear on each plate): **MPC79A**

FIELD POLARITIES of the plates, the MASK LABELS, and the CD widths should be as follows:

Plate Name	Plate Field	Plate Label	CD Widths (see color plate for locations)
DIF	OPAQUE	XEROX DIF A1	5.0 μm
IMP	CLEAR	XEROX IMP A2	5.0 μm
POL	OPAQUE	XEROX POL A3	5.0 μm
CUT	CLEAR	XEROX CUT A4	5.0 μm
MET	OPAQUE	XEROX MET A5	5.0 μm
PAD	CLEAR	XEROX PAD A6	5.0 μm

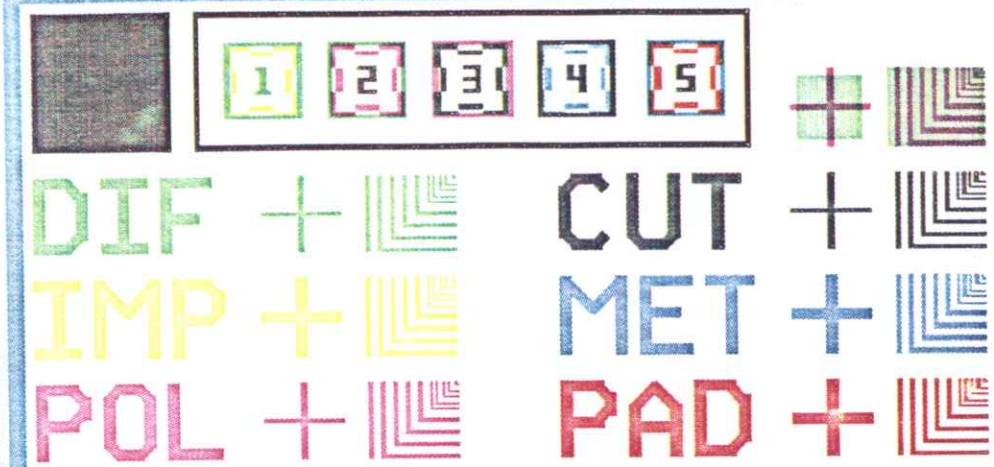


Wafer Layout Map: MPC79A

(Die size: 7696 x 6477 microns)

+ marks center of wafer

(WaferMapA.Sil)

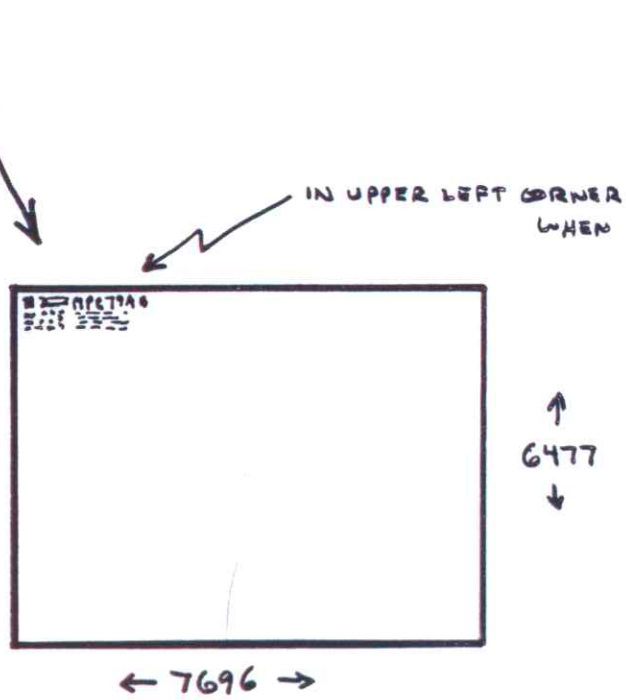


MPC79AG

1979 Multi-University Project Chip

Info Mgmt: Xerox PARC/SSL
Data Comm: ARPANET
Masks by: Micro Mask, Inc
Wafer Fab: Hewlett-Packard/ICPL

CD's:



CRITICAL DIMENSION LOCATOR MAP

```
SLICE   1,13
DTITLE  A,MPC79A
MTITLE  01,DIF
MTITLE  02,IMP
MTITLE  03,POL
MTITLE  04,CUT
MTITLE  05,MET
MTITLE  06,PAD
OPTION  B,M,P01,P03,P05
CHIP    01,(A,EBCL000-01-CP)
ROWS    18415/50800
ROWS    50800/18016;83584
ROWS    83185/50800
CHIP    02,(01,MPC79AB-10-DI)
$          (02,MPC79AB-20-IM)
$          (03,MPC79AB-30-PO)
$          (04,MPC79AB-40-CU)
$          (05,MPC79AB-50-ME)
$          (06,MPC79AB-60-PA)
ROWS    70231/35408,5,7696
ROWS    76708/35408,5,7696
CHIP    03,(01,MPC79AC-10-DI)
$          (02,MPC79AC-20-IM)
$          (03,MPC79AC-30-PO)
$          (04,MPC79AC-40-CU)
$          (05,MPC79AC-50-ME)
$          (06,MPC79AC-60-PA)
ROWS    50800/27712,3,7696
ROWS    57277/27712,3,7696
ROWS    63754/27712,3,7696
CHIP    04,(01,MPC79AD-10-DI)
$          (02,MPC79AD-20-IM)
$          (03,MPC79AD-30-PO)
$          (04,MPC79AD-40-CU)
$          (05,MPC79AD-50-ME)
$          (06,MPC79AD-60-PA)
ROWS    57277/50800,4,7696
ROWS    63754/50800,4,7696
CHIP    05,(01,MPC79AE-10-DI)
$          (02,MPC79AE-20-IM)
$          (03,MPC79AE-30-PO)
$          (04,MPC79AE-40-CU)
$          (05,MPC79AE-50-ME)
$          (06,MPC79AE-60-PA)
ROWS    37846/27712,4,7696
ROWS    44323/27712,4,7696
CHIP    06,(01,MPC79AF-10-DI)
$          (02,MPC79AF-20-IM)
$          (03,MPC79AF-30-PO)
$          (04,MPC79AF-40-CU)
$          (05,MPC79AF-50-ME)
$          (06,MPC79AF-60-PA)
ROWS    37846/58496,3,7696
ROWS    44323/58496,3,7696
ROWS    50800/58496,3,7696
CHIP    07,(01,MPC79AG-10-DI)
$          (02,MPC79AG-20-IM)
$          (03,MPC79AG-30-PO)
```

```
$          (04,MPC79AG-40-CU)
$          (05,MPC79AG-50-ME)
$          (06,MPC79AG-60-PA)
ROWS    24892/35408,5,7696
ROWS    31369/35408,5,7696
CHIP    08,(01,MPC79AH-10-DI)
$          (02,MPC79AH-20-IM)
$          (03,MPC79AH-30-PO)
$          (04,MPC79AH-40-CU)
$          (05,MPC79AH-50-ME)
$          (06,MPC79AH-60-PA)
ROWS    50800/20016;50800;81584
CHIP    09,(A,EBCL000-02-CP)
ROWS    18415/50800
ROWS    50800/18016;83584
ROWS    83185/50800
END
```

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, CA 94304
December 3, 1979
5

To: Micro Mask, Inc.

From: Alan Bell (494-4326), Reference: P.O. #40784

Subject: MEBES Master Plate Specifications for project: **MPC79B**

Max. Pattern Dimensions : X: 7696 μm Y: 6477 μm
Step and Repeat distances: X: 7696 μm Y: 6477 μm

# Plates per Set:	6	Defect Density:	Standard
Plate Material:	Chrome, L.E. 30	Tolerance:	+/- 0.25 μm
Plate Size:	4" x 4" x 0.60"	CD width:	(see below)
E-beam Spot Size:	0.50 μm	Oversizing:	None
Pattern Size:	3", Round	Undersizing:	None

Pattern Specifications: There are seven (7) different project dies (named I, J, K, L, M, N, O) in this mask set. All have identical dimensions (7696 x 6477 microns). See the diagram on the following pages for the placements of die types within the mask set, and for the location of the CD's. For the purposes of this description, the six master plates will have the following plate names: DIF, IMP, POL, CUT, MET, PAD. The dies will be supplied on magtape in MEBES format.

Filenames for each layer are given in the following table (file names as a function of mask level/die type):

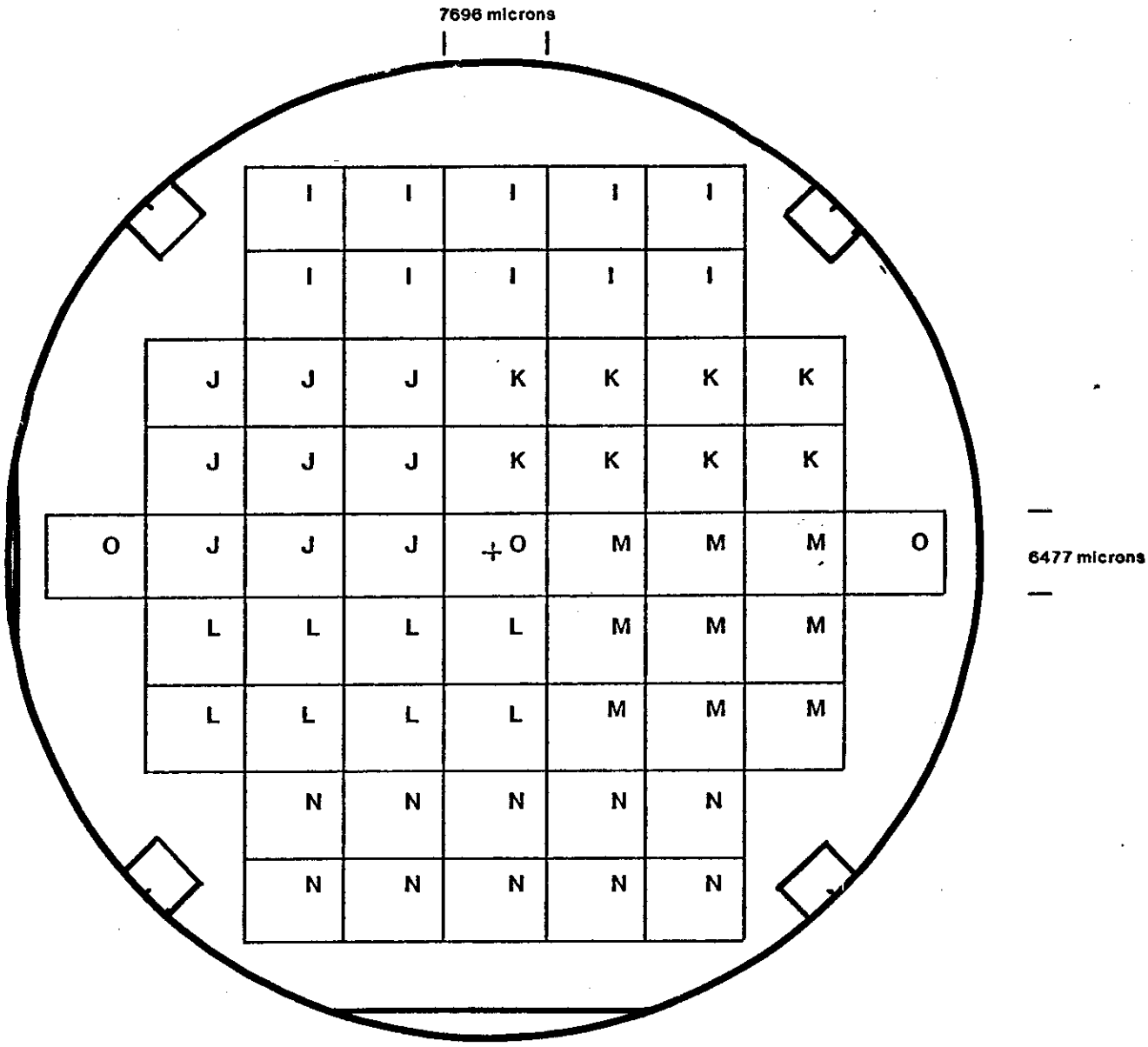
	DIF	IMP	POL	CUT	MET	PAD
Die I:	MPC79BI-10-DI	MPC79BI-20-IM	MPC79BI-30-PO	MPC79BI-40-CU	MPC79BI-50-ME	MPC79BI-60-PA
Die J:	MPC79BJ-10-DI	MPC79BJ-20-IM	MPC79BJ-30-PO	MPC79BJ-40-CU	MPC79BJ-50-ME	MPC79BJ-60-PA
Die K:	MPC79BK-10-DI	MPC79BK-20-IM	MPC79BK-30-PO	MPC79BK-40-CU	MPC79BK-50-ME	MPC79BK-60-PA
Die L:	MPC79BL-10-DI	MPC79BL-20-IM	MPC79BL-30-PO	MPC79BL-40-CU	MPC79BL-50-ME	MPC79BL-60-PA
Die M:	MPC79BM-10-DI	MPC79BM-20-IM	MPC79BM-30-PO	MPC79BM-40-CU	MPC79BM-50-ME	MPC79BM-60-PA
Die N:	MPC79BN-10-DI	MPC79BN-20-IM	MPC79BN-30-PO	MPC79BN-40-CU	MPC79BN-50-ME	MPC79BN-60-PA
Die O:	MPC79BO-10-DI	MPC79BO-20-IM	MPC79BO-30-PO	MPC79BO-40-CU	MPC79BO-50-ME	MPC79BO-60-PA

PLEASE adjust the patterns so that the TEXT on the mask is WRONG-READING when viewed from the CHROME SIDE.

DEVICE LABEL (to appear on each plate): **MPC79B**

FIELD POLARITIES of the plates, the MASK LABELS, and the CD width should be as follows:

Plate Name	Plate Field	Plate Label	CD Widths (see color plate for locations)
DIF	OPAQUE	XEROX DIF B1	5.0 μm
IMP	CLEAR	XEROX IMP B2	5.0 μm
POL	OPAQUE	XEROX POL B3	5.0 μm
CUT	CLEAR	XEROX CUT B4	5.0 μm
MET	OPAQUE	XEROX MET B5	5.0 μm
PAD	CLEAR	XEROX PAD B6	5.0 μm

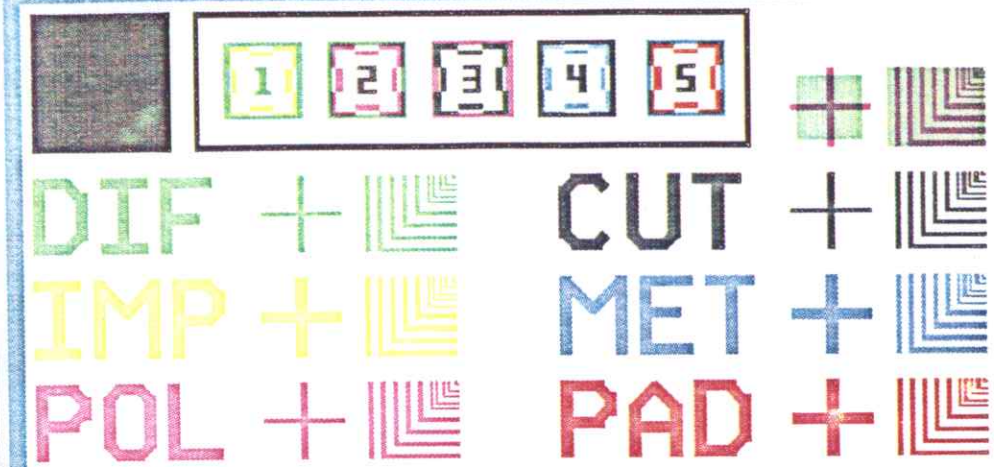


Wafer Layout Map: MPC79B

(Die size: 7696 x 6477 microns)

+ marks center of wafer

(WaferMapB.sil)

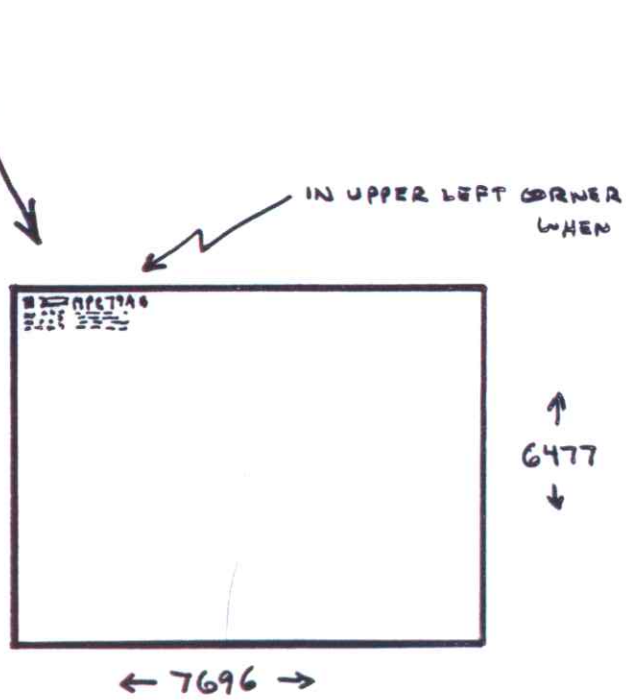


MPC79AG

1979 Multi-University Project Chip

Info Mgmt: Xerox PARC/SSL
Data Comm: ARPANET
Masks by: Micro Mask, Inc
Wafer Fab: Hewlett-Packard/ICPL

CD's:



CRITICAL DIMENSION LOCATOR MAP

MPC79 HP Letters:

HEWLETT hp PACKARD

3500 Deer Creek Road, Palo Alto, California 94304, U.S.A., Telephone 415 494-1444, TWX 910 373 1267

FROM: Mike Beaver

DATE: December 31, 1979

TO: MPC 79 Distribution

SUBJECT: MPC 79 Wafer Data

The attached data on the initial two runs for MPC79 represents in-process data from test wafers generated in the normal course of wafer fabrication plus electrical measurements taken on one of the wafers from each lot. This data is enclosed to give you some benchmark data against which you can compare your actual test results. Most of the electrical data was taken with a curve tracer and is subject to appropriate tolerances.

Additionally, wafer to wafer variations exist. If you need more precise data, you can generate it by probing the test devices on the border of each chip.

The follow-on run, from which you may receive additional chips will be similarly characterized. If you have specific questions about the processing, I will attempt to answer them.

Mike

Hewlett-Packard's Participation in MPC-79

The wafer fabrication segment of MPC-79 was performed by the Integrated Circuit Processing Laboratory of Hewlett Packard Co. which fabricated the MPC-78 project last year. This lab, directed by P. L. Castro, gives HP Labs the capability to do silicon wafer processing utilizing a wide range of modern processes and processing techniques. The NMOS process selected for MPC-79 utilizes more routine and standardized techniques and is optimized for ease of manufacture rather than density. This gave the highest probability of providing working circuits to the MPC-79 participants within the 2-3 week turnaround time that is basic to the MPC concept. In order to insure proper scaling of device dimensions as they were translated from design as-drawn dimensions to mask dimensions and finally to as-processed dimensions, HP-ICPL provided the needed information on the dimensional shifts that occur in the photomasking and etching operations. This information, together with the agreed upon valve of λ (2.5 microns) was used to properly alter the pattern data sent to the maskmaker. The resulting mask sets were used to produce two runs each of the two different mask sets, all of which were within the expected range for DC parameters and all of which provided working chips.

An annotated listing of the process follows. Certain minor steps, such as cleaning have been omitted from the listing for compactness.

Operation	Comment
Stress-Relief Oxidation	Thin oxide to separate the nitride fron the silicon
Nitride Deposition	Silicon Nitride layer deposited by Low Pressure Chemical Vapor Deposition
Diffusion Mask	This step defines and etches the nitride layer. The resulting nitride pattern defines the active (diffusion) areas.
Field Oxidation	Only the field is oxidized, isolating the active areas from each other. Again the nitride acts as a mask.
Field Implant	This implant is blocked from the active areas by the nitride. This implant raises the threshold of parasitic (field) transistors.
Nitride Strip	The masking nitride is removed
Gate Oxidation	A very clean gate oxide is grown

Enhancement Implant	Sets threshold for enhancement mode devices
Depletion Implant Mask	Defines which transistors will be depletion mode (load) devices. The photoresist itself is used to block the implant from the remainder of the wafer
Depletion Implant	Sets depletion mode device threshold
Poly Deposition	Poly silicon is deposited by Low Pressure Chemical Vapor Deposition
Poly Oxidation	The surface of the poly is oxidized
Poly Mask	Defines the poly areas
Source/Drain Predep	Provides doping for the transistor sources and drains. The poly protects the gate regions from being doped
N Oxidation	Drive-in and oxidation for source/ drain areas
Oxide Deposition	Low Pressure Chemical Vapor Deposition oxide deposited to provide additional insulation between poly and metal lines
Contact Mask	Opens contacts to diffusion and poly levels
Al-Si Evaporation	Metal fil deposition
Metal Mask	Defines and etches metal layer
Alloy	Alloy contacts to poly and diffusion levels to provide low resistance conduction paths
Plasma Nitride	Plasma deposited nitride layer for passivation (optional)
Pad Mask	Opens holes to bonding pads through plasma nitride

In addition to the actual wafer fabrication, electrical testing of the test pattern devices was performed to verify process parameters. Scribing and a limited amount of packaging of chips was also done at Hewlett Packard. The measured parameters are listed on the next page.

Run #	KDEI1	KDEI2	KDEI3	KDEI4
Mask Series	A	B	A	B
Thresholds (v) (recalculated)				
Enhancement	1.0	1.0	1.1	1.2
Depletion	4.6	3.9	3.9	3.8
Poly Field	21	20	16	21
Metal Field	21	20	14	20
Resistances (kΩ)				
Poly Resistor	6.4	8.4	6.7	7.0
Diffusion Resistor	3.6	3.9	3.2	3.6
Poly-Metal Contacts	2.3	2.6	2.1	2.15
Diff-Metal Contacts	1.4	1.4	1.0	1.1
Butting Contacts	3.6	4.3	3.15	3.2
Diffusion-Substrate Breakdown (v)	35.0	34.5	34.0	34.0
Osc Frequency @ 5 v	17.0	17.7	14.6	14.8
Process Parameters				
Gate Oxide Thickness Å	990	1000	1030	1040
Field Oxide Thickness Å	14600	14600	15400	14850
Poly Thickness Å	5370	5300	5040	4910
Intermediate Oxide Thickness Å	5000	5400	5100	5100
Diffusion Sheet Resistance Ω/□	17.2-17.8	16.2-17.1	16.3-17.0	16.4-17.3

The value of λ chosen for MPC-79 (2.5μ) was the result of a compromise between ease of processing, particularly masking operations, and density. A smaller value of λ could have been chosen but this was not considered to be a good balance of benefit and risk. The possibility of reducing λ for 1980 projects is being considered. Continued progress in reproducable etching techniques at Hewlett Packard (and the rest of the industry) should help to keep the risk low and processing time at a minimum.

HP-ICPL is happy to have participated in this joint project designed to greatly reduce the cycle time, from circuit design through packaged parts, of complex integrated circuits. We plan to work with the MPC Team for 1980 while plans are made to establish an industrial capability for fast turn-around processing in future years.

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
Palo Alto, CA 94304
January 14, 1980

Merrill Brooksby
Hewlett-Packard
1501 Page Mill Road
Palo Alto, CA 94304

Dear Merrill:

The effort to implement the fall '79 integrated system design projects for the universities has worked out very well. A total of 82 projects from 124 designers are included in the multiproject chip set. Many major projects have already been tested and several important ones have proven to work correctly. I've enclosed a short document which will give you and your colleagues an overview of the effort, some information on the participants, and a feeling for how things turned out.

It is my hope that MPC79 will serve as a powerful demonstration of the feasibility and the capability of fast-turnaround VLSI implementation, and thus confirm your early vision of how valuable such a service would be to the community of designers.

All of us here at PARC who participated in this effort want to thank you for your very valuable assistance in setting up the collaborative arrangements between Xerox PARC/SSL and HP-ICPL. None of this would have happened without your help these past two years.

Sincerely,

Lynn Conway

Lynn Conway
Manager, LSI Systems Area

MPC79 Gray Letters:

OFFICE OF THE CHANCELLOR

CAMBRIDGE, MASSACHUSETTS 02139

March 7, 1980

Mr. David T. Kearns
President
Xerox Corporation
Stamford, Connecticut 06904

Dear Mr. Kearns:

As you know, a number of universities participated, during the past six months, in the demonstration operation of a prototype system for remote-entry, fast-turnaround implementation of very large-scale integrated circuit designs. This collaboration was organized and implemented by members of the Systems Science Laboratory at the Xerox Palo Alto Research Center.

The Massachusetts Institute of Technology was one of the university participants in this demonstration experiment, and twenty seven students and members of the faculty, mostly in the Department of Electrical Engineering and Computer Science, had the opportunity to submit designs which were fabricated through this project and returned to them for testing and evaluation before the start of the next academic term. This opportunity to learn the technique of VLSI design, to apply those techniques to a real problem and to see the tangible results of that design process, all in a single term, provides the basis for an extraordinarily effective and rich educational experience. Thus, the 1979 Multi-University Multiproject Chip-Set experiment has made major contributions here both to the ongoing educational process, and to our active plans for developing at M.I.T. a fast-turnaround VLSI capability. I am sure that the project will have benefits for industries which use VLSI technology as well, both in terms of the contribution it makes to graduates who are competent in these techniques, and in terms of its strengthening of the Institute's capabilities in this area.

My purpose in writing about this project is simply to express to you, on behalf of the Institute and those who participated in the project here, our gratitude and appreciation for the generous support for this activity which Xerox has provided. This important project would not have been possible without the leadership provided by Xerox through its Palo Alto Research Center. In this regard, I would particularly like to acknowledge the extraordinary efforts of Lynn Conway, whose determination and leadership made all the necessary pieces come together.

Thank you very much.

Sincerely yours,

Paul E. Gray
Chancellor

PEG:jls
cc: George E. Pake
W. R. Sutherland

OFFICE OF THE CHANCELLOR

CAMBRIDGE, MASSACHUSETTS 02139

March 7, 1980

Mr. John A. Young
President
Hewlett-Packard
1501 Page Mill Road
Palo Alto, California 94304

Dear Mr. Young:

As you know, a number of universities participated, during the past six months, in the demonstration operation of a prototype system for remote-entry, fast-turnaround implementation of very large-scale integrated circuit designs. This collaboration was organized and implemented by members of the Systems Science Laboratory at the Xerox Palo Alto Research Center.

The Massachusetts Institute of Technology was one of the university participants in this demonstration experiment, and twenty seven students and members of the faculty, mostly in the Department of Electrical Engineering and Computer Science, had the opportunity to submit designs which were fabricated through this project and returned to them for testing and evaluation before the start of the next academic term. This opportunity to learn the technique of VLSI design, to apply those techniques to a real problem and to see the tangible results of that design process, all in a single term, provides the basis for an extraordinarily effective and rich educational experience. Thus, the 1979 Multi-University Multiproject Chip-Set experiment has made major contributions here both to the ongoing educational process, and to our active plans for developing at M. I. T. a fast-turnaround VLSI capability. I am sure that the project will have benefits for industries which use VLSI technology as well, both in terms of the contribution it makes to graduates who are competent in these techniques, and in terms of its strengthening of the Institute's capabilities in this area.

My purpose in writing about this project is simply to express to you, on behalf of the Institute and those who participated in the project here, our gratitude and appreciation for the generous support for this activity which Hewlett-Packard has provided. Your willingness to fabricate the wafers used in this project both without charge and with the priority attention required to accommodate the very tight time schedule was a critical factor in the success of the program. The efforts of Patricia Castro, Director of your IC Processing Laboratory, and her personal interest in this project, were very significant factors in its success.

Thank you very much.

Sincerely yours,

Paul E. Gray
Chancellor

PEG:jls

OFFICE OF THE CHANCELLOR

CAMBRIDGE, MASSACHUSETTS 02139

March 7, 1980

Mr. Joseph C. Ross, Jr.
Chairman and President
Micro Mask, Incorporated
695 Vaqueros Avenue
Sunnyvale, California 94086

Dear Mr. Ross:

As you know, a number of universities participated, during the past six months, in the demonstration operation of a prototype system for remote-entry, fast-turnaround implementation of very large-scale integrated circuit designs. This collaboration was organized and implemented by members of the Systems Science Laboratory at the Xerox Palo Alto Research Center.

The Massachusetts Institute of Technology was one of the university participants in this demonstration experiment, and twenty seven students and members of the faculty, mostly in the Department of Electrical Engineering and Computer Science, had the opportunity to submit designs which were fabricated through this project and returned to them for testing and evaluation before the start of the next academic term. This opportunity to learn the technique of VLSI design, to apply those techniques to a real problem and to see the tangible results of that design process, all in a single term, provides the basis for an extraordinarily effective and rich educational experience. Thus, the 1979 Multi-University Multiproject Chip-Set experiment has made major contributions here both to the ongoing educational process, and to our active plans for developing at M.I.T. a fast-turnaround VLSI capability. I am sure that the project will have benefits for industries which use VLSI technology as well, both in terms of the contribution it makes to graduates who are competent in these techniques, and in terms of its strengthening of the Institute's capabilities in this area.

My purpose in writing about this project is simply to express to you, on behalf of the Institute and those who participated in the project here, our gratitude and appreciation for the generous support for this activity which Micro Mask, Incorporated has provided. Your willingness to expedite the preparation of the masks required in this project, in order to accommodate the extremely-tight time schedule was a critical factor in the success of the program.

Thank you very much.

Sincerely yours,

Paul E. Gray
Chancellor

PEG:jls

MPC79 Kearns' Letter:

Xerox Corporation
Stamford, Connecticut 06904

Office of the President

XEROX

March 17, 1980

Dear Chancellor Gray:

Thank you for the words of appreciation expressed in your March 7 letter concerning MIT's participation in the 1979 Multiproject Chip experiment conducted under the leadership of Lynn Conway and the auspices of our Palo Alto Research Center.

Our research scientists and engineers are, for their part, indebted to the students and faculty who have cooperated so helpfully in making these experiments an all-around success. Without widespread participation of the university community, it would be more difficult for us in Xerox to validate our efforts to improve greatly the techniques for fast turnaround implementation of VLSI, and for training our own engineers and scientists in these new technologies.

We are of course gratified that MIT finds the effort as worthwhile as Xerox does, and we look forward to future synergies between our research and univeristy research.

Sincerely,

David T. Kearns

DTK/mps

c: G. E. Pake
W. R. Sutherland

Chancellor Paul E. Gray
Massachusetts Institute of Technology
Cambridge, Massachusetts 02139